
Curriculum Vitæ
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Sarma Vrudhula is a Professor in the School of Computing, Informatics and Decisions Systems Engineering at Arizona State University, Tempe AZ. He received the B.Math (Honors) from the University of Waterloo, Ontario, Canada, in 1976 and his M.S. and Ph.D degrees in electrical engineering from the University of Southern California in 1980 and 1985, respectively. During 1985-1992 he was on the faculty of the EE-Systems department of the University of Southern California. From 1992 to 2005 he was a professor in the Electrical and Computer Engineering department at the University of Arizona, in Tucson, AZ.

In 1996 he established the NSF Center for Low Power Electronics (CLPE) at the University of Arizona, in collaboration with the EE department of the Arizona State University. CLPE was supported by the NSF, the State of Arizona, and many leading companies in the microelectronics industry. Through CLPE, he has facilitated the research of twenty faculty and over 40 graduate students across both campuses. He is also the founding director of the NSF I/UCRC Center for Embedded Systems at ASU.

He holds 10 patents, and has authored or co-authored more than 220 papers in top tier journals and conferences in several areas in design automation and computer aided design for digital integrated circuit and systems, focusing on low power design and energy management of circuits and systems. His active areas of research include: new circuit architectures of threshold logic circuits for the design of ASICs and FPGAs; technology mapping with threshold logic circuits; the implementation of threshold logic using spintronic devices, and non-Boolean computation in emerging technologies, hardware acceleration of convolutional and deep neural networks, constructive synthesis of neural networks, recurrent neural networks; energy optimization of battery powered computing systems and wireless sensor networks; system level dynamic power and thermal management of multicore processors and system-on-chip (SoC); statistical methods for the analysis of process variations; statistical optimization of performance, power and leakage. His teaching experience includes both undergraduate and graduate courses in digital systems design and testing, VLSI design, CAD algorithms for VLSI, advanced synthesis and verification methods, computer architecture, and discrete mathematics.

He has served on the technical program committees of many national and international conferences in VLSI design automation and CAD, and on government review panels. He served as an Associate Editor for the IEEE Transactions on VLSI, and is presently an Associate Editor for the IEEE Transaction on CAD, and the ACM Transactions on Design Automation of Electronic Systems (TODAES). During the 2000-2001, he was a visiting scientist with the Advanced Design Tools group in Motorola, Austin.

Recognitions: He was made Fellow of the IEEE in 2016 for “*contributions to low power and energy-efficient design of digital circuits and systems.*”, and elected as member of National Academy of Inventors in 2017. He has received three best paper awards (2017, 2016, 2008), an outstanding paper award (2001) and a best researcher (CS department internal) award (2011).

Education

- B.Math** Mathematics and Computer Science, 1976
University of Waterloo, Waterloo, Canada.
- M.S.** Electrical Engineering, 1981
University of Southern California, Los Angeles.
- Ph.D.** Electrical Engineering, 1985
University of Southern California, Los Angeles.

Employment

- Feb. '09 - Present** Director, NSF IUCRC Consortium for Embedded Systems
- Jan. '05 - Present** Professor, Computer Science and Engineering Dept.,
Arizona State University, Tempe AZ.
- Apr. '96 - Dec. '04** Director, NSF S/IUCRC Center for Low Power Electronics
University of Arizona, Tucson, AZ.
- Apr. '96 - Dec. '04** Professor, Electrical and Computer Engineering Dept.
University of Arizona, Tucson, AZ
- Aug. '92 - July '96** Associate Professor, Electrical and Computer Engineering Dept.
University of Arizona, Tucson, AZ
- Jan. '85 - Aug. '92** Assistant Professor, Dept. of Electrical Engineering-Systems
University of Southern California, Los Angeles, CA.
- Sept. '81 - Dec. '84** Research Assistant, Dept. of Electrical Engineering-Systems
University of Southern California, Los Angeles, CA.
- Apr. '82 - Sept. '82** Member of Technical Staff, IBM, Hopewell Junction, NY.
- June '78 - Sept. '81** Member of Research Staff, USC Information Sciences Institute
Marina Del Rey, CA.
- Sept. '76 - Sept. '77** Member of Technical Staff, Bell Canada, Toronto, Canada.

- Elected member of *National Academy of Inventors*, 2017.
- *IEEE Fellow*, for “contributions to low power and energy-efficient design of digital circuits and systems”, 2016.
- *Best Paper Award*: “*Statistical Library Characterization Using Arbitrary Polynomial Chaos*”, Mehmet Ince, Sule Ozev and Sarma Vrudhula, 8th Latin American Symposium on Circuits and Systems, Bariloche, Argentina, March 2017.
- *Best Paper Award*: “*Digital IP Protection Using Threshold Voltage Control*”, with Joseph Davis, Niranjan Kulkarni, Jinghua Yang, Aykut Dengi. International Symposium of Quality Electronic Design (ISQED), 2016.
- *Outstanding Researcher*: School of Computing, Informatics and Decision Systems Engineering, ASU, 2010.
- *Best Researcher*: (Senior Faculty), School of Computing, Informatics and Decision Systems Engineering, ASU, 2011.
- *Best Paper Award*: “A methodology for characterization of large macro cells and IP blocks considering process variations”, with Amit Goel, Feroze Taraporevala, Praveen Ghanta. International Symposium of Quality Electronic Design (ISQED), 2008.
- *Outstanding Paper Award*: for “Performance Driven Placement and Routing for Field Programmable Analog Arrays”, with Haibo Wang and Olek Palusinski. International Conference on Mixed Design of Integrated Circuits and Systems, Zakopane, Poland, 2001.

Journals

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 - *New Approaches to Reducing Power and Areas of ASICs*, Federal University of Rio Grande do Sul, Institute of Informatics, Department of Applied Informatics, May 2, 2018.
 - *Embedding Threshold Logic into ASICs and FPGAs for Improving Performance, Power and Area*, Distinguished Speaker, Electrical and Computer Engineering Department, Texas A&M University, Colleague Station, TX, April 9, 2018.
 - *Non-Conventional Approaches to High Performance, Low Power Digital Circuits*, National Reconnaissance Office, August 16, 2017.
 - *A Clock Skewing Strategy to Reduce Power and Area of ASIC Circuits*, IEEE Design Automation Conference, June 22, 2017.
 - *Integrating Threshold Logic with ASIC Design*, Maxlinear Inc., April 7, 2017.
 - *Statistical Library Characterization using Arbitrary Polynomial Chaos*, Latin American Symposium on Circuits and Systems, February 22, 2017.
 - *Reducing Power, Leakage and Area of Standard-Cell ASICs using Threshold Logic Flip-flops*, Globalfoundries, Bangalore India, December 21, 2016.
 - *Energy Management of Thermally Constrained Multicore Processors*, Samsung Semiconductor, Inc., Austin Texas, October 18, 2016.
 - *Energy Efficient Design and Energy Management of Digital Systems*, Faculty Seminar Series, School of Computing, Informatics and Decisions Systems Engineering, Arizona State University, April 15, 2016.
 - *ASIC Design using Threshold Logic*, Mentor Graphics, March 18, 2016.
 - *Design of Threshold Logic Gates using Emerging Devices*, Special Session on “Device-Circuit-System Integration Using Emerging Memory Part-II Session”, International Symposium on Circuits and Systems (ISCAS), Lisbon, Portugal, May 25, 2015.
 - *Reducing Power, Leakage and Area using Threshold Logic Gates*, National University of Singapore, Jan. 25, 2014.
 - *C-Programmable Coarse-Grain Reconfigurable Hardware Accelerator: Architecture for a Signal Processing Co-Processor*, Raytheon Missile Systems, Tucson, AZ, Feb. 24, 2014.
 - *Spintronic Threshold Logic Array (STLA): A Compact, Low Leakage, Non-Volatile Gate Array Architecture*,
 - Everspin Inc., Chandler AZ, Jan. 25, 2013.
 - Qualcomm, Inc. San Diego, CA, Feb. 1, 2013.
 - *Reliable Design with Unreliable Components*, NSF/SRC/DFG Joint Workshop on “Bugs and Defects in Electronic Systems: The Next Frontier”, April, 22, 2013.

- *Digital Design using Threshold Logic Cells*
 - Texas Instruments Inc., July 15, 2013.
 - Broadcom Inc., Nov. 26, 2013
- *Energy Efficient Computing, **Keynote Talk*** at IEEE International Conference on Computer Systems and Industrial Informatics (ICCSII), Sharjah, United Arab Emirates, Dec. 18-20, 2012.
- *Spintronic Threshold Logic Array (STLA) A Compact, Low Leakage, Non-Volatile Gate Array Architecture*, NANOARCH 2012, Amsterdam, Netherlands, July 5, 2012.
- *Thermal Aware Performance Optimization of Multicore Processors*, Karlsruhe Institute of Technology, Karlsruhe, Germany, July 2, 2012.
- *Digital Design with Threshold Logic*
 1. Karlsruhe Institute of Technology, Karlsruhe, Germany, July 2, 2012.
 2. Qualcomm Inc., San Diego CA, May 31, 2012.
 3. Airforce Research Laboratory, Kirtland Airforce Base, Albuquerque, NM, March 23, 2012.
- *A Balanced 4-Moduli Set and its Reverse Converter Design for Efficient FIR Filter Implementation*, Great Lakes VLSI Symposium, Ecole Polytechnique, Lasusanne Switzerland, April 11, 2011.
- *Boosting Performance per Watt*
 1. Qualcomm Inc., San Diego CA., Sept, 9, 2010.
 2. Granite Ventures Inc., Phoenix AZ, Feb. 12, 2010.
 3. Cypress Semiconductor Inc., San Jose CA, June 4, 2011.
 4. Texas Instruments Inc., Dallas TX, June 6, 2011.
- *Multicore Thermal Management*, Intel Inc. Chandler, AZ, Feb 05, 2010.
- *Design space exploration and dynamic thermal management of multicore processors*,
 1. NSF Workshop on the Science of Power Management, April 9, 2009.
 2. AMD Inc., Santa Clara, CA., Nov 12, 2008.
- *Multicore performance optimization under thermal constraints*, Microsoft Corp., Seattle, WA., May 1, 2008.
- *A unified approach to statistical analysis of full-chip leakage and timing in the presence of process variations, **invited talk*** given at Broadcom Inc., Irvine, CA., Aug. 19, 2008.
- *Performance optimization of multi-core processors under thermal constraints, **Invited Talk*** given at

1. Seoul National Univeristy, South Korea, Jan. 25, 2007.
 2. Microsoft Inc., Seattle, Washington, Sept. 14, 2007.
 3. Intel Corp., Chandler Arizona, Sept. 20, 2007.
- *Statistical Analysis of Leakage and Timing*, **Keynote Talk** given at 3rd Annual CLEAN (Controlling LEAorage power in NanoCMOS SOC's) Workshop, Gothenburg Sweden, Sept. 6, 2007.
 - *Computation of Joint Timing Yield of Sequential Networks considering Process Variations*, International Workshop on Power And Timing Modeling, Optimization and Simulation (PAT-MOS), Sept. 3, 2007, Goteborg, Sweden.
 - *Analysis of Leakage and Timing in the presence of process variations*, LSI Logic Inc., Aug. 30, 2007.
 - *Robust design of nano-scale circuits in the presence of process variations*, Full-day tutorial given at the IEEE International Conference on VLSI Design, Bangalore, India, Jan 7, 2007.
 - *Stochastic Analysis of interconnects and power grids in the presence of process variations*, First International Workshop on Interconnect Design and Variability, Bangalore, India, Dec. 28-29, 2006.
 - 3-Day Tutorial, Texas Instruments, Bangalore, Dec. 19-21, 2006.
 - VLSI Circuit Simulation - Dec. 19, 2006
 - Deterministic Static Timing Analysis - Dec. 19, 2006
 - Source & Impact of Process Variations - Dec. 20, 2006
 - Statistical Models of Interconnects & Gates - Dec. 20, 2006
 - Statistical Timing & Leakage Analysis - Dec. 21, 2006
 - Optimization in the presence of process variations - Dec. 21, 2006
 - *Methodology for the robust design of nano-scale circuits in the presence of process variations*, Freescale Inc., Austin TX, May 17, 2006.
 - *Statistical timing and leakage analysis in the presence of process variations*, Freescale Inc., Austin TX, May 17, 2006.
 - *Energy Management in Battery Powered Embedded Systems*, EECS Dept., University of Michigan, Ann Arbor, MI Mar. 2004.
 - *Analysis and Optimization of Power and Performance of Digital Circuits and Systems*, ST Microelectronics, Phoenix, AZ, Feb. 2004.
 - *Statistical Approach to Signal Integrity and Performance Analysis of DSM CMOS Circuits*, Connection One, Arizona State University, Jan. 2004.
 - *Battery-Aware Design of Portable Embedded Systems*, **Distinguished Speaker**, Embedded Systems Research Center (ESRC), Seoul National University, Aug. 28, 2003.

- *Identification of the Minimum Leakage States*, Cadence Inc., San Jose CA, Oct. 2003.
- *Statistical Gate Sizing to Improve Timing Yield*
 - Cadence Inc., San Jose CA, Oct. 2003.
 - TAU Workshop, Austin TX, Feb. 2004.
- *Approaches to Minimizing Subthreshold Leakage*, Mindspeed Inc., Irvine CA, June 2003.
- *Energy Management in Battery Powered Embedded Systems*, IBM ARL, Austin, TX, June 2003.
- *Probabilistic Analysis of Interconnect Coupling Noise in Deep Submicron Circuits*
 - **Distinguished Speaker**, Silesian University of Technology, Gliwice, Poland, June 2001.
 - **Distinguished Speaker**, University of Mining and Metallurgy, Akademia Gorniczo-Hutnicza, June 2001.
 - Motorola Inc., Austin TX, Aug. 2001.
 - Center for Low Power Electronics (nationally broadcast), Oct. 2001.
- *Algorithms for Minimizing Standby Power in Dual VT CMOS Circuits*
 - Intel Corp., Santa Clara, CA, Sept. 1999.
 - Intel Corp., Portland Oregon, Sept. 1999.
 - Sun Microsystems, San Jose, CA Aug. 2000.
 - **Distinguished Speaker**, Silesian University of Technology, Gliwice, Poland, June 2000.
 - **Distinguished Speaker**, University of Mining and Metallurgy, Akademia Gorniczo-Hutnicza, June 2000.
 - Center for Low Power Electronics (nationally broadcast), Apr. 2000.
- *Synthesis Algorithms for Low Power Digital Systems*, Cadence Inc., San Jose, CA 1998
- *Dynamically Reconfigurable Architectures: Opportunities and Challenges*, Panel Session (Chair) International Conference on Computer Design (ICCD), Austin, TX, Oct. 1998.
- *Low Power Electronics: Digital Circuits. Keynote Speaker* at the Hughes Low Power/Low Voltage Symposium, Newport Beach, CA, Mar. 20, 1997.
- *Rewiring of Combinational and Sequential Logic for Low Power*, Department of Electrical Engineering, University of Michigan, Ann Arbor, Michigan, Sept. 1997.
- *Techniques for Power Reduction in Combinational and Sequential Logic Circuits*, Mentor Graphics, May 1997.
- *Power Optimization of Combinational and Sequential Logic Circuits*, IBM Hopewell Junction, New York, June 1997.
- *Center for Low Power Electronics*, IBM, Hopewell Junction, NY, June 1997.

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- *Register Transfer Level Testing using Edge Valued Binary Decision Diagrams*, Viewlogic Inc., Fremont, CA., Oct. 1996.
 - *Edge Valued Binary Decision Diagrams*, International Dahsthul Seminar on Computer-Aided Design and Test, Feb. 1995, Dagstuhl, Germany.
 - *Edge Valued Binary Decision Diagrams with Applications to Logic Verification, Synthesis, Spectral Transforms, and Combinatorial Optimization*
 - Fujitsu Laboratories of America, San Jose, CA., Apr. 1995,
 - Electrical Engineering Department, University of California Irvine, CA., May 1995.
 - *A Fast and Accurate Technique for Estimating Signal Activity in CMOS Logic Circuits*, Motorola Inc., Chandler AZ., Feb. 1995.
 - *Asynchronous Systems Design Methodology*. ECE Department, University of Arizona, Tucson, AZ., Feb., 1995.
 - *Low Power Design at the Logic, Register-Transfer & Behavior Levels*. Motorola Inc, Chandler, AZ., Apr. 1994.
 - *Synthesis of Asynchronous Systems from Data Flow Specifications*. IBM, Austin, TX, Aug. 19, 1993 and at IBM Rochester, Minn., Nov. 1993.
 - *Design and Test for VLSI*. Department of Atomic Energy, Minerals Division, Hyderabad, Andhra Pradesh, India, Dec. 1992.
 - *Modelling Fault Propagation for Predicting Fault Coverage and Test Length*. Indian Institute of Technology, New Delhi, India, Dec. 1992.
 - *Stochastic Models for Testability Analysis of Digital Circuits*. Department of Electrical Engineering, University of Arizona, Apr. 1992.
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 - *A Branching Process Model for Fault Propagation in Combinational Circuits*. Pacific Northwest Test Workshop, Seattle, Washington, 1991.
 - *Stochastic Models in Testing of Digital Circuits*. MCC, Austin Texas, Sept. 1990.
 - *Testability Analysis and Characterization of Digital Circuits*. Department of Electrical Engineering, UC Irvine, Mar. 1990.
 - *LARA : A Layout Accelerator Based on the Reduced Array Architecture*. Department of Computer Science and Automation, Indian Institute of Science, Bangalore, India, Aug. 1988.
 - *Statistical Properties of Partitioning and Floorplanning Problems*. Department of Computer Science and Automation, Indian Institute of Science, Bangalore, India, Aug. 1988.

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- *Minority Fellowship Awards in Science for Undergraduates*. TRW, El Segundo, CA, Oct. 1987.
- *On Mapping Algorithms to Linear and Fault Tolerant Systolic Arrays*. IEEE International Conference On Computer Design, Port Chester, New York, Oct. 1986.
- *Wireability Analysis of Integrated Circuits*. Hewlett Packard Research Labs., Palo Alto, CA, Dec. 1985.
- *A Metric-Free VLSI Layout Language*. IBM General Technology Division, Hopewell Junction, New York, Aug. 1982.

1. Jinghua Yang, *Embedding Logic and Non-volatile Devices in CMOS Digital Circuits for Improving Energy Efficiency*, Ph.D. Electrical Engineering, April 2018.
2. Timothy Rauschenbach, *A Simulation Framework of Blockchain*, Baretts Honors Thesis, Computer Science and Engineering, 2017.
3. Benjamin Gaudette, *An Intelligent Framework for Energy-aware Mobile Computing Subject to Stochastic System Dynamics*, Ph.D. Computer Engineering, 2017.
4. Kody Stribny *Mobile Waterway Monitor: Boyant and Dynamic Waterway Sensing*, Barretts Honors Thesis, 2017.
5. Niranjana Kulkarni *Energy-Efficient Digital Circuit Design using Threshold Logic Gates*, Ph.D. Computer Science, 2016.
6. Mahdi Hamzeh *Compiler and Architecture Design for Coarse-Grained Programmable Accelerators*, Ph.D Computer Science, 2015.
7. Digant Desai *Towards Energy Efficient Computing with Linux : Enabling Task Level Power Awareness and Support for Energy Efficient Accelerator*, MS Computer Science, 2013.
8. Vinay Hanumaiah *Unified Framework for Energy-Proportional Computing in Multicore Processors: Novel Algorithms and Practical Implementation*, Ph.D, Electrical Engineering, 2013.
9. Yang Hu, *Testing of threshold logic latch based hybrid circuits*, MS, Electrical Engineering, 2013.
10. Benjamin Gaudette, *Energy Management in Solar Powered Wireless Sensor Networks*, MS Computer Science, 2012.
11. Tejaswi Lingegowda, *Threshold Logic Properties and Methods: Applications to post-CMOS Design Automation and Gene Regulation Modeling*, Ph.D. 2011
12. Samuel Leshner, *Modeling and implementation of threshold logic circuits and architectures*, Ph.D 2010
13. Gayathri Chalivendra, *A new RNS 4-moduli set for implementation of FIR filters*, MSEE 2011
14. Saurabh Patel, *Improving resilience against differential power analysis with low area and power overhead using threshold logic*, Saurabh Patel, MSEE, 2010
15. Amit Goel, *Characterization of nanoscale digital circuits for statistical timing and signal integrity analysis*, MSEE 2008.
16. Ravishankar Rao, *Fast and accurate techniques for early design space exploration and dynamic thermal management of multi-core processors*, Ph.D. Electrical Engineering, 2008.
17. Sudheendra Kadri, *Performance driven design space exploration in portable devices powered by fuel cell battery hybrid system*, MSEE 2007.

18. Praveen Ghanta, *Stochastic performance modeling and analysis of VLSI circuits in the presence of process variations*, Ph.D. 2007.
19. Sarvesh Bhardwaj, *Novel techniques for analysis and optimization of nano-scale digital circuits in the presence of process variations*, Ph.D. 2006
20. Ravishankar Rao, *Energy Optimal Speed Control for Components of Portable Systems*, MSEE 2004.
21. Sreeja Raj, *Statistical Timing Analysis*, MSEE 2004.
22. Sridhar Dasika, *Energy Management of Sensor Networks*, MSEE 2004.
23. Kaviraj Chopra, *Symbolic Algorithms for Identifying Minimum and Bounded Leakage States*, MSEE 2004.
24. Raghukiran Sreeramaneni, *Energy Profiler for Hardware-Software Codesign*, MSEE 2003.
25. Sarvesh Bhardwaj, *Analysis of Functional and Delay Noise due to Coupling*, MSEE 2003.
26. Daler Rakhmatov, *Energy Optimization for Portable, Battery Powered Systems*, Ph.D. 2002.
27. Haibo Wang, *Field Programmable Analog Array Synthesis*, Ph.D. 2002.
28. Qi Wang, *Logic Synthesis for Low Power*, Ph.D. 1999.
29. Daler Rakhmatov, *Dynamic Scheduling in Runtime Reconfigurable Systems*, MSEE 1998.
30. Yukti Bareja, *RTL Level Power Estimation*, MSEE 1998.
31. Thomas J. Brown, *Algorithms for Clustering of Dataflow Graphs for Implementation on Dynamically Configurable FPGAs*, MSEE 1998.
32. David Rutishauser, *Object Oriented Simulation of a GPS Receiver*, MSEE 1998.
33. Bryce A. Rasmussen, *A Design of a Counterflow Pipeline Processor*, MSEE 1997.
34. Kendel McCarley, *Design of an High Performance Asynchronous Floating Point Unit*, MSEE 1996.
35. Edwin Tsun, *Design of an High Performance Asynchronous RISC Processor*, MSEE 1996.
36. Tzyh-Yung Wu, *Automatic Synthesis of Asynchronous Systems from Data-Flow Specifications*, Ph.D. 1995.
37. Hong-Yu Xie, *Gate Level Power Estimation*, MSEE 1995.
38. Oliver Harquin, *Asynchronous Discrete Cosine Transform Processor*, MSEE 1995.
39. King C. Ho, *A Graph Theoretic Approach for Two Dimensional Topological Compaction of Regular VLSI Structures*, Ph.D. 1994.
40. Ang Li, *Partitioning for Pseudo Exhaustive Built-In Self-Test*, MSEE 1991.

Dissertation/Thesis Committees (as Chair)

41. Yung-Te Lai, *Logic Verification and Synthesis using Function Graphs*, Ph.D. 1993.
42. Amitava Majumdar, *Stochastic Models for Testing of Digital Circuits*, Ph.D. 1992.
43. Ravikumar Chennagiri, *Parallel Algorithms and Architectures for Physical Design of VLSI Circuits*, Ph.D. 1991

Arizona State University:

- University Tenure and Promotion Committee, 2016-2019.
- Search Committee for Director of CIDSE, 2016-2017.
- Undergraduate Program Committee for CSE, 2014-2014, 2015-2016, 2016-2017.
- Graduate Program Committee for CENG, 2013-2014, 2014-2015, 2015-2016, 2016-2017.
- Search Committee for Dean of Fulton School of Engineering, 2015-2016.
- Chair, Faculty Recruiting Committee, *Next Generation Computing*, 2012-2013, 2013-2014, 2014-2015.
- Director of Research, Consortium for Embedded Systems, 2005 -
- Chair, Computer Engineering Program Committee, Fulton School of Engineering, 2009-
- Graduate Program Committee, Committee, Computer Science and Engineering, 2008-2010.
- Personnel Committee, Computer Science and Engineering, 2005-2007.
- Chair, Faculty Recruiting Committee, Committee, Computer Science and Engineering, 2005.
- Academic Senate, Arizona State University, 2005-2006.

University of Arizona:

- Promotion & Tenure Committee, Electrical and Computer Engineering Department, 2002-2004.
- Director Summer Internship Program (SPIN) for CLPE, 1996-2004.
- Chair, Faculty Recruiting Committee, Electrical and Computer Engineering Dept., 1997-1998, 2000-2003.
- Computer Engineering Faculty Recruiting Subcommittee, 1993-1994, 1996.
- Undergraduate Curriculum Committee, Electrical and Computer Engineering Dept., 1996-1997.
- Graduate Student Recruiting and Awards Committee, Electrical and Computer Engineering Dept.
- Computer Engineering Curriculum, Electrical and Computer Engineering Dept., 1992-1993, 1996-1997.
- Peer Evaluation Committee, Electrical and Computer Engineering Dept., 1995-1997.
- Chair, Computer Policy Committee, Electrical and Computer Engineering Dept., 1993-1996.
- International Graduate Admissions, Electrical and Computer Engineering Dept., 1994-1996.

Journal Editorships, Program and Other Committees

- IEEE Fellow Committee, 2017.
- Associate Editor *IEEE Transactions on Multi-Scale Computing Systems (TMSCS)*, 2015-2016.
- Associate Editor *IEEE Transactions on Computer-Aided Design (TCAD)*, 2006-2013.
- Associate Editor *ACM Transactions on Design Automation of Electronic Systems (TODAES)*, 2006-2009.
- Associate Editor *IEEE Transactions on VLSI Systems*, 1996-1998.
- Member of Editorial Board, *Studia Informatica*, Silesian University of Technology Press, Gliwice, Poland, 2001-2002.
- Member of the Board of Directors: Computer Systems Support Solutions, 1998.
- External Reviewer, Computer Engineering Program, Southern Illinois University, Carbondale, 2002.
- Program Committee Member:
 - *Symposium on Biomorphic Circuits & Systems with Threshold Logic*, (BioTL) 2014.
 - *IEEE/ACM International Symposium on Nanoscale Architectures (NANOARCH)*, 2014.
 - *IEEE International Symposium on Low Power Electronic Design (ISLPED)*, 2014.
 - *IEEE International Conference on Computer Aided Design (ICCAD)*, 2014.
 - *IEEE International Conference on Computer Aided Design (ICCAD)*, 2013.
 - *IEEE/ACM Design Automation Conference*, 2001-2004, 2014.
 - *IEEE International Conf on Embedded Software and Systems*, China. 2005.
 - *International. Symposium on Quality Electronic Design (ISQED)*, 2003-2006.
 - *Mixed Design of Integrated Circuits and Systems*, Poland, 2000-2001.
 - *Southwest Symposium on Mixed-Signal Design*, 1999.
 - *International Conference on Computer Design (ICCD)*, 1993-1997.
 - *NSF S/IUCRC Symposium at the University of Oklahoma*, 1997.
- Chair, Vice-Chair, Organizer Positions:
 - *Organizer of Special Session on “Toward On-Chip Cortical Computing”*, IEEE/ACM Design Automation Conference (DAC), Sanfrancisco, CA, June 2014.
 - *Organizer of Special Session on “Neuron Inspired Computing using Nanotechnology”*, 9th Asia and South Pacific Design Automation Conference (ASP-DAC), Singapore, 2014.
 - *Chair Technical Program Committee (RDIC)*, *International. Symposium on Quality Electronic Design (ISQED)*, 2005-2006.

- *Chair* Technical Program Committee (Power), IEEE/ACM Design Automation Conference, 2005-2006.
- *Organizer* and *Chair* of Special Session on “Error Tolerant Design”, IEEE/ACM Design Automation Conference, 2005.
- *Session Chair*, Sensor Networks and Communication Systems, International. Symposium on Low Power Electronic Design (ISLPED), Seoul, Korea, 2003.
- *Chair*, *National Science Foundation S/IUCRC Symposium*, 1999.
- *Vice Chair*, *IFIP Working Group on Hardware/Software co-Design*, 1998.
- *Track Chair*, *IEEE International. Conference on Computer Design (ICCD)*, 1998.
- *Organizer and Session Chair on Dynamically Reconfigurable Architectures*, IEEE International. Conference on Computer Design (ICCD), 1998.
- *VLSI/VHSIC Session Chair*, *Phoenix Conference on Computers and Communications*, 1993.
- General Chairman of *Second International Workshop on The Economics of Design and Test*, 1993.
- Reviewing and Refereeing
 - Invited External Reviewer for the Portuguese National Science Foundation
 - IEEE International Conference on Computer Design
 - IEEE International Conference on Computer-Aided Design
 - IEEE International Conference on Computers and Communications
 - IEEE VLSI Test Symposium
 - IEEE Design Automation Conference
 - Journal of Electronic Testing and Test Applications
 - ACM Transactions on Design Automation
 - IEEE Transactions on VLSI Systems
 - IEEE Transactions on CAD
 - Journal of Integrated Computer-Aided Engineering
 - IEE Proceedings
 - Proposals for the National Science Foundation