

Dr. Sayfe Kiaei
School of Electrical, Computer and Energy Engineering
Arizona State University, Tempe, AZ 85287

Motorola Endowed Chair Professor in Analog and RFIC
Director, NSF IUCRC Center Connection One
Director, Center for Advance Studies in Energy (USPCASE)
Email: Sayfe at asu edu

FIELDS OF SPECIALIZATION

Analog / Digital Integrated Circuits, Radio Frequency Integrate Circuits, Sensors, Bio-Electronics, Power Management IC, Communication Systems, Wireless and Wireline Communication System

ACADEMIC AND INDUSTRIAL POSITIONS

2001-Present: Professor, Motorola Endowed Chair Professor in Analog and RFIC - Director of Connection One NSF Center, School of Electrical, Computer, and Energy Engineering, Arizona State University, Tempe, AZ

- **Professor:** Research and teaching in integrated circuits, RF circuits and systems, Communications, Wireless and Wireline transceiver, mixed-signal and Analog IC, Sensors, Power management IC.
- **Director and PI:** Partnership Center for Energy systems, funded by USAID, \$18M.
- **Research Projects:** funded by NSF, USAID, DARPA, JPL, NASA, Motorola Inc., Intel Inc., Broadcom, Qualcomm, Raytheon, General Dynamics, Texas Instruments, and over 10 other industries. Areas: IC design, Analog and digital IC, Power Management IC, RFIC, Wireless and wireline transceivers, Sensors, hearing aid circuits and systems, and related area. Current significant research awards:
 - Partnership Center for Energy systems, USAID, 2015-2020, \$18M. Principle Investigator
 - QESST NSF ERC Center on Solar Energy, NSF, 2010-2020, \$36M, Co-PI, Test-bed Director
 - Solar Energy Development in ME, Private funds and World Bank, \$1.5M
 - Connection One NSF Center, Director, NSF and Industry, Center annual expenditure over \$5 M

2015-Present: Director, Center for Advance Studies in Energy (USPCASE)

Director of ASU USAID funded USPCASE program. The project funded by the USAID is a partnership between Arizona State University and two leading Pakistani universities: the National University of Sciences and Technology (NUST) and the University of Engineering and Technology (UET) Peshawar. The focus is on applied research relevant to Pakistan's energy needs and help produce skilled graduates in energy fields. An \$18 million award supports the project — the largest ASU has ever received from USAID. Dr. Kiaei is the director for the program. <https://uspcase.asu.edu/>

2004-Present, Director of NSF IUCRC Center Connection One, School of Electrical, Computer, and Energy Engineering, Arizona State University, Tempe, AZ

NSF Connection One Industry/University Cooperative Research Center. Established the center in 2002 with focus on Integrated Circuits and Systems, including wireless system, RF, and related areas. The center has five

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universities with over 30 industrial members. The center has over 12 faculty members, with annual funding over \$5M. www.connectionone.org

2008-2012: Associate Dean of Research, Ira A. Fulton Schools of Engineering, Arizona State University

Responsible for leading the research infrastructure, promoting and developing research programs with industry and federal agencies, leading large multi-university proposals, investing and providing seed funding to foster new research areas, and promoting graduate program in the college of engineering. Research Enterprise support included:

- College funding grew from \$50M to over \$80M in 2012 while Dr. Kiaei was the Associate Dean.
- Established the first NSF Engineering Research Center (ERC) at the ASU on Solar Energy. Dr. Kiaei managed, organized and planned the ERC proposal process. ASU is the lead school partnering with MIT, Georgia Tech, U of Delaware, Cal-Tech, U of New Mexico, and UA.
- Lead several trans-disciplinary 4M research projects (4M: multi-million, multi-investigator, multi-disciplinary, multi-university grants) in energy, security, and related initiatives.
- Assisted in the development of several new Research Centers in the college.
- Oversight of over 20 existing research centers in the college of engineering.
- Working with Vice President for Research, Dean's, and directors on University-wide research initiatives.
- Engage with industry and federal government to establish new research collaborations.
- Organized workshops and supported proposals for NSF, NIH, DOE, DOD, DARPA, etc.
- Organized workshops for new assistant professors to apply for NSF CAREER Awards. ASU CAREER awards grew from 3 annual awards in 2008 to over 10 in 2010.
- Annual budget over \$7M for supporting research centers, seed funding for new center, cost sharing, proposal support, equipment and infrastructure support, graduate scholarships, and research administration. ADR Staffs included, Director of industrial and government liaison, Director of research administration, and 14 research advancement staff, Project manager responsible for supporting large projects and proposals, Director of graduate programs recruitment and scholarships, Technical writer for supporting proposals, Research and academic data analysis
- Research Administration and pre-award proposal administration for the schools. Developed a decentralized research administration and advancement team for the Schools supporting 5 schools, 12 departments, over 220 engineering faculty, with funding over \$70M.
- Graduate Programs: Recruiting, Fellowships, marketing, outreach, coordination with departments

1993-2002: Motorola Inc., Senior Member of Technical Staff, Personal Communication Sector, Austin, Texas, and Plantation, FL. Worked at several sectors on projects related to wireless communications, two way radios, wireless networks, ADSL and MODEM, RF, and related areas. Projects included:

- **Cellular Division**, WITC: Wireless Technology Center. Responsible for wireless handset development, including 2G, 3G, 4G Bluetooth, WIFI transceiver, GPS Receiver, wireless networks, and related areas. Managed a group for the development of GPS IC, 3G baseband IC, Bluetooth IC, and various subcomponents of RF front-end circuits and systems.
- **ADSL Group**, System & Architecture Engineering, Broadband Products Operations, responsible for ADSL, MODEM, OFDM, Broadband Wireline System, broadband wireless communication transceivers, Development of a single chip mixed-signal ADSL transceiver (*CopperGold™*). The transceiver contained Analog Front End (A/D, D/A, Hybrid), DMT, modulation/demodulation, FFT, IFFT, echo canceler, time

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domain equalizer, front-end constellation mapping, Trellis code modulation, Viterbi decoder) and an on-chip DSP core.

- **Land Mobile Products Sector**, Plantation FL, responsible for Wireless digital two-way radios, hot spot wireless network, next generation of digital two-way radios, "*Talk about Radios*", Japanese cellular systems (PHS).
- **University relations:** Responsible for the development of collaborative research programs with several universities. Responsible for funding research in the areas of Wireless Transceiver IC Design, RF, and mixed-signal and baseband system architecture.
- **Standards:** Technical representative of Motorola in the standards meetings including 2G-4G, GPS, Bluetooth, and DSL standards including T1E1, International Telecommunication Unit (ITU), ETSI, 3GPPP, Universal ADSL Working Group (UAWG), etc.

1995-2002, Adjunct Professor, Electrical and Computer Engineering Dept., The University of Texas, Austin, Texas

- Taught graduate courses at UT Austin on Introduction to Telecommunication System and Digital Communications. Co-advised two Ph.D. program committees in IC design and Telecomm (while at Motorola)

1987-1993, Assistant / Associate Professor (Tenured) Electrical and Computer Engineering Department, Oregon State University, Corvallis, OR

- Research and classes in Electronics, DSP, Communication system and networks, Wireless systems, MODEMS. Graduated 30 MS and Ph.D. students.
- Faculty Chair, Computer Engineering Program, Developed a new Computer Engineering Program at OSU in 1987
- Co-Director, National Science Foundation Center for the Design of Analog/Digital IC's (CDADIC),. CDADIC is a NSF center focused on mixed-signal IC research. CDADIC members include four universities (*Oregon State University, University of Washington, Washington State University, University of N.Y. Stony Brook*), over 25 Electronics companies, and the National Science Foundation.

1985-87: Member of Research Staff, Boeing Co., Bellevue, Wa, Flight Systems Research and Technology Center, summer. Design Engineer, Hardware and CAD tool development for system control.

DEGREES

- **Ph.D.**, Electrical and Computer Engineering, Washington State University, 1987
- **M.S.**, Electrical and Computer Engineering, Washington State University, 1984
- **B.S.E.E., Electrical Engineering, Northeastern University/WSU, 1982**

AWARDS

- IEEE Fellow

Dr. Sayfe Kiaei
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- IEEE Fellows CAS Committee Chair, 2009-2012
- Global Standards Award, For contributions in the International Telecommunication Unit (ITU) for Asymmetric Digital Subscriber Line (ADSL) G.Lite Standards. Motorola Inc., 1999.
- 10X Cycle Reduction Award, for development of new IC design process from DSP algorithm to IC layout, Motorola Inc., 1995.
- IEEE Darlington Award, IEEE Circuits and Systems Society Best Paper Award, 1995. For “Characterization and Comparison of CMOS FSCL Circuits with Conventional CMOS for mixed-signal ICs,” Published at: *IEEE Trans. on Circuits and Systems II, Sept. 93*.
- Carter Best Teaching Award, College of Engineering Best Teacher Award, Oregon State University, 1992. For “*outstanding and inspirational teaching in the College of Engineering*”. Award is selected by the confidential vote of all of the undergraduate students in the College of Engineering among over 125 professors in the College.
- Industrial University Fellowship (IUF) Award, *National Science Foundation*, 1993.
- Research Initiation Award, *National Science Foundation*, 1990-93.
- Outstanding Graduate Student Scholarship, *Azur-Data Inc. WSU*, 1984

FUNDED RESEARCH PROJECTS

Summary of annual Research Awards at ASU, 2002-Present:

2002	2003	2004	2005	2006	2007	2008	2009	2010	2011	2012	2013	2014	2015
\$255K	\$644K	\$1.85M	\$1.2M	\$1.35M	\$650K	\$840K	\$650K	\$640K	\$1.5M	\$1.2M	\$950K	\$2.25M	\$3.2M

Partial list of Research Awards:

- USAID, PCASE – Center for Energy systems, 2015-2020, \$18M. PI and Director
- NSF, QESST NSF ERC Center on Solar Energy, 2010-2020, \$36M, Kiaei, Co-PI, Testbed Director,
- Private Donor, \$1.5M, 2012-2015, Solar Energy Development
- NSF IUCRC Center, Connection One 2002-present, \$3.5M as PI, over \$5M annual center fund with other faculty in the center.
- NSF, Micro-Power Multi-Phase MEMS Hearing Aid, 2007-2011, \$500K
- NSF - Design for Implantable Bio-Sensors, 2007-2009, \$480K
- Science Foundation of AZ, PEPER- Photovoltaic Environmental Performance and Reliability for the Arizona-Wide Electric Grid, 2009-2013, \$1.2M
- SRC –Self Characterization for Calibration and Process Feedback of MEMS Devices, 2011-2014, \$300K
- NSF- Cognitive MIMO Communications for Dynamic-Spectrum Wireless Networks – 2012-2014, \$150K
- NSF, Autonomous Self-Healing Sensor Network Radio, 2010-2014, \$250K
- DARPA, Neural-Enabled Prostheses with Sensorimotor Integration, \$500K

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- NSF, Microwave Sensors for Vital Signs Monitoring Device Design, 2011-2013, \$250K
- NSF, Various REU funds, 8/31/12-8/31/13, \$400K
- DARPA, Nano-Mechanical RF Band pass resonator for 2GHz RF Applications, with JPL, \$2.2 M, 2002-2005,
- Qualcomm, Connection One Center, Various projects funded for the center, 2005-Present, \$1.2M
- Texas Instruments, Various projects 2009-present, \$1.5M
- *Motorola Inc.*, Various projects 2002-2010, \$1.2M.
- *SIRF Technologies*, GPS Transceiver, 2005, \$300K.
- *Ridgetop Inc.*, RF Harsh Environment, \$200K
- Freescale Semiconductor, PWM Power Management, 2006, \$150K
- State of Arizona, *WINTeCH- Wireless Integrated Nano Technology Center Support* (2005-2009), Ranging from 450K annually from 2005-2009.
- BAE Systems; “New Techniques for Time Measurement Circuits LiDAR; 2005-2008; \$650K
- SRC (Semi-conductors research Corp), Ultra-Wideband Transceivers, \$225K, 2001-2003
- Intel Corporation, Design of Multi-Standard RF Front-End Circuits, \$300K, 2002-2005
- *National Science Foundation*, Adaptive Compensation of Analog circuits imperfections using DSP methods, \$150K, 1996 (tie project with UC San Diego NSF center), 2010-2011
- Center for the Design of Analog/Digital IC’s (CDADIC) 1987-1995, At Oregon State, \$1.5M
- Low Power IF processing for Direct Digital Transceivers, *Motorola Inc*, \$100K, 93.
- Hewlett-Packard Faculty Chair position in Mixed-Signal IC, HP, 1995-97, \$500K
- *National Science Foundation, Motorola Inc.* Faculty Industry Fellowship, \$250K, 93-94.
- *National Science Foundation, Research Initiation Award (RIA) (same as current CAREER Award)*, Synthesis and Automatic Derivation of Multi-Rate VLSI Arrays for DSP Algorithms, , 90-93. \$320K.
- CDADIC, various projects on Low-Noise Source Coupled Logic (SCL), Mixed-Mode IC's, *CDADIC* \$350K, 1988-1992.
- Decimation Filters for A/D Noise Enhancements, Tektronix, Inc., \$100K, 1988.
- Various grants for IC Fabrication (DARPA/MOSIS, VLSI), testing equipment (Tek, HP), DSP system development (TI, Motorola), ranging in various amounts up to \$200K/year. At Oregon State, 1988-1997.

CONSULTANT

- Intel Inc. Chandler, AZ, 2002-2006: Development of 3G-4G Wireless transceiver.
- Sony Inc., San Diego, CA and Tokyo, Japan, 2002-2004: Review and development of various telecom cellular system architecture including 3G system architecture, and GPS system.
- Motorola Inc. 2002-2005: Supporting development of DSL, E911, GPS integrated circuits and systems for the cellular and mobile handsets.

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- Hewlett Packard, Corvallis, OR – 1990-1993: Various project on development of custom analog and digital IC's for printer and inkjet system. Some of this work was under consultation, and some under various research grants with Oregon State University.
- Tektronix Inc, Beaverton, OR - 1988-1990: Design and Implementation of Data acquisition system for Spectrum analyzer, development of custom DSP algorithm for the Tektronix spectrum analyzer including system architecture, simulation, analysis, and design of oversampled data acquisition system.
- Boeing Commercial Aircraft, BCAC, Renton, WA - 1985-1987: Development of Airplane Controller Model, Simulation and Implementation of Flight control, Model reduction, and system control.

EXPERT WITNESS (Patent, IP)

Patent litigation, patent validity, IPR, expert reports, deposition, testimony, and trade secrets in the following areas (Complete list of cases available):

- Analog and Digital IC, Radio Frequency Integrated Circuits, Power Management, Power Management IC
- Wireless communication, Communication networks, Signal Processing, Communication system,
- Hearing AID, Bio-Electronics, Heart monitoring system, Bi-sensors
- Standards including AMPS, GSM, CDMA, WCDMA, LTE, 1G, 2G, 3G, 4G, BT, WiFi (802.11), DOCIS, and related ITU/ETRI/3G.PPP standards.
- Satellite communications, Satellite Transceiver, ECHO and Multi-path cancelation circuits
- Wireline Communications, MODEM, Digital Subscriber Line, ADSL, VDSL, MODEM
- Wireless LAN, Wi-Fi, 802.11, Bluetooth. ZIGBEE
- GPS system, GPS receiver.
- MEMS, Bulk Acoustic Wave Filters, SAW, MEMS resonators, MEMS accelerometer Signal Processing, Communication Systems.

PROFESSIONAL RECOGNITION

- IEEE Fellow, 2002-Present
- IEEE Fellow Committee Chair, CAS, 2008-2010
- IEEE Fellow Committee member, 2007-2010.
- IEEE Senior Member, 1993-Present, IEEE Member 1987-1992.
- IEEE Faculty Advisor, Oregon State University, 1987-1990

IEEE Editorials

- IEEE Microwave Magazine, Guest Editor,
- IEEE System Journal, Associate Editor, 2010-2011.
- Associate Editor, IEEE Transactions on VLSI, Jan 2001-2008.

Dr. Sayfe Kiaei
School of Electrical, Computer and Energy Engineering
Arizona State University, Tempe, AZ 85287

- IEEE Comm. Magazine, guest Editor, Feature Issues on “Circuits for Wireless and Wireline Communications,” April 1999.
- IEEE Transactions on Microwave Theory and Techniques , Guest editor, Special Issue on: "Radio Frequency IC Design,” Dec. 1998.
- IEEE Transactions on Circuits and Systems-II , guest editor, Special Issue on: “Low-Power Wireless Communication Systems,” June 1997.
- Associate Editor, IEEE Transactions on Circuits and Systems-II, 1993-1996.
- *Editor and Reviewer for IEEE ASIC/SOC Conference,*
- *Editor and Reviewer for IEEE Microwave Theory and Techniques Journal*
- *Editor and Reviewer for International Journal of Analog Integrated Circuits and Signal Processing*
- *Founding member of IEEE RF Integrated Circuits Symposium*
- *Associate Editor, IEEE Communications, Tutorial & Surveys Magazine, 2006-2009.*

Conference Organizations

- RFIC Executive Committee members, 2000-present, Steering Committee Member, RFIC symposium, 1996-Present.
- RFIC Founding member, 1995-96.
- Technical Program Chair, IEEE International Sym. on Circuits and Systems, Phoenix, AZ, 2002.
- ISSCC Admin Council, Conferences Committee 2000-2005.
- General Chair, Radio Frequency IC (RFIC) Symposium, Seattle, WA, 2002.
- Technical Program Chair, RFIC Symposium, Phoenix, AZ, 2001.
- Finance Chair, RFIC symposium, Boston, MA, 2000.
- Publicity Chair, RFIC symposium, Los Angeles, CA, 1999.
- Transactions Chair, RFIC symposium, Baltimore, MD, 1998.
- General Chair, Int. Sym. on Low-Power Electronics and Design (ISLPED), Monterey, CA, 97.
- Executive Committee Member, Int. Symp. On Low-Power Electronics and Design, 96-2000.
- Technical Program Committee Member of the following conferences:
 - International Conference on Circuits and Systems: 1996, 2000, 2001, 2004-2008
 - RFIC Symposium, 1996-Present
 - Application Specific Array Processing (ASAP): 2000-2002
 - Technical Program Chair, Int. Sym. on Low-Power Electronics and Design, Monterey, CA, 96.
 - Arizona Telecom Comm (ATIC)
 - GLS VLSI 1998, Lafayette, Louisiana, 1998
 - VLSI Design 98, Chennai, India, Jan. 1998.
 - ICECS, Lisbon, Portugal, 98.
 - Application Specific Array Processing, 1995-97, 2000
 - Vehicular Technology Conference, 1995-97.

Dr. Sayfe Kiaei
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- Inter. Conf. on Intelligent Information Systems, D.C., 1994-95.
- IEEE Pacific Rim Conference on Communications & Computers, Victoria, BC, Canada, 1991.

Invited talks, Panelist, Session Chairs, Workshop Speaker

- Conference chair, Technical Program committee chair and TPC member, tutorials, workshops, session chair, etc. in RFIC, ISSCC, ISCAS, VLSI, ICASSP, Low-Power Symposium, ICC, Application Specific IC's, IMS, MTT, etc.

PATENTS, PUBLICATIONS

Patents & Disclosures

1. Finite impulse response digital to analog converter, US Pat. 7528754 -
2. Oscillator frequency correction in GPS signal acquisition, US6661371B2
3. Efficient non-iterative frequency domain method and system for ..., US Pat. App 11489102
4. Monolithic supply-modulated RF power amplifier and DC-DC power ..., US Pat. 7372333
5. Compressed vector-based spectral analysis method and system for ..., US Pat. App 10535616
6. Integrated ZVS synchronous buck DC-DC converter with adaptive control, US Pat. 7218085
7. Low-Noise MOS Folded Source Coupled Logic (FSCL) for Mixed-Signal ICs" US 5,149,992.

Patent applications

1. S. Kiaei, N. Darbanian, Shahin Farahani, .S. Provisional Application No. 60/428,432, # 51579P/DMC/A59, " CVB RF Models.
2. "Circuits and Systems for Powers of Two Wave Digital Filters," Motorola Inc., 1995
3. "Direct Digital Demodulation for Narrow band signals," Motorola Inc., 1996
4. "Capacity Maximized TEQ block for ADSL", Motorola Inc., 97.
5. "Fast LMS Equalization with adaptive step size for TEQ," Motorola Inc., 98.
6. "Peak-to-Average (PAR) reduction for DMT system," Motorola Inc., 98.

Standards Contributions

1. "Spectral Compatibility of ADSL: Frequency Overlap vs. FDM," T1E1, Dec. 97.
2. "Echo Cancellation for G.Lite Universal ADSL," Universal ADSL Working Group, Atlanta, GA, Jan 98.
3. "8-bit QAM Constellation effects on reach for universal ADSL," Universal ADAL Working Group, Atlanta, GA, Jan 98.
4. "Trellis Code Modulation coding gain," Universal ADAL Working Group, Atlanta, GA, Jan 98.
5. "Monte Carlo Modeling and simulation of twisted pair wiring," Universal ADAL Working Group, Atlanta, GA, Jan 98.
6. "Overlap Upstream/Downstream spectral allocation for ADSL," International Telecommunication Unit, Chicago, March 98.
7. "Echo Cancellation for ADSL," International Telecommunication Unit, Antwerp, Belgium, 98.
8. "Performance of Echo Cancellation ADSL system in the presence of Near End Cross Talk (NEXT)," International Telecommunication Unit, Honolulu, Hawaii, June 98.

Dr. Sayfe Kiaei
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9. Presentations and editorials at various ADSL standards: ITU, UAWG, and T1E1, 97-99.

Books

“Design, Modeling and Testing of Data Converters, P Carbone, S Kiaei,” F Xu - 2014 – Springer, © Springer-Verlag Berlin Heidelberg 2014

Refereed Journal Papers

1. Marti-Arbona, E.; Mandal, D.; Bakkaloglu, B.; Kiaei, S., "A High-Voltage Compliant Current-to-Digital Sensor for DC-DC Converters in Standard CMOS Technology," *IEEE Transactions on Power Electronics*, no. 99, 2016
2. Chang, D.; Kitchen, J.N.; Bakkaloglu, B.; Kiaei, S.; Ozev, S., "Monitor-Based In-Field Wearout Mitigation for CMOS LC Oscillators," in *IEEE Transactions on Device and Materials Reliability*, vol. 16, no. 2, pp. 183-193, 2016.
3. Chang, D.; Kitchen, J.N.; Bakkaloglu, B.; Kiaei, S.; Ozev, S., "Design-Time Reliability Enhancement Using Hotspot Identification for RF Circuits," in *IEEE transactions on Very Large Scale Integration (VLSI) Systems*, -vol. 24, no. 3, pp. 1179-1183, 2016
4. Seungkee Min; Copani, T.; Kiaei, S.; Bakkaloglu, B., "A 90-nm CMOS 5-GHz Ring-Oscillator PLL With Delay-Discriminator-Based Active Phase-Noise Cancellation," *Solid-State Circuits, IEEE Journal of*, vol.48, no.5, pp.1151,1160, May 2013
5. Junghan Lee; Tino Copani; Terry Mayhugh Jr.; Bhaskar Aravind; Sayfe Kiaei; Bertan Bakkaloglu., "A 280 mW, 0.07% THD+N class-D audio amplifier using a frequency-domain quantizer," *Analog Integrated Circuits and Signal Processing*, 173-186, 2012.
6. Seungkee Min; Copali, T.; Kiaei, S.; Bakkaloglu, B.; , "A 90nm CMOS 5GHz ring oscillator PLL with delay-discriminator based active phase noise cancellation," *Radio Frequency Integrated Circuits Symposium (RFIC), 2012 IEEE*, pp. 173-176, 2012
7. Deligoz, I.; Naqvi, S.R.; Copani, T.; Kiaei, S.; Bakkaloglu, B.; Sang-Soo Je; Junseok Chae; , "A MEMS-Based Power-Scalable Hearing Aid Analog Front End," *Biomedical Circuits and Systems, IEEE Transactions on*, vol.5, no.3, pp.201-213, June 2011
8. Copani, T.; Seungkee Min; Shashidharan, S.; Chakraborty, S.; Stevens, M.; Kiaei, S.; Bakkaloglu, B.; , "A CMOS Low-Power Transceiver With Reconfigurable Antenna Interface for Medical Implant Applications," *Microwave Theory and Techniques, IEEE Transactions on*, vol.59, no.5, pp.1369-1378, May 2011
9. Khalil, W.; Shashidharan, S.; Copani, T.; Chakraborty, S.; Kiaei, S.; Bakkaloglu, B.; , "A $700\text{-}\mu\text{A}$ 405-MHz All-Digital Fractional- N Frequency-Locked Loop for ISM Band Applications," *Microwave Theory and Techniques, IEEE Transactions on*, vol.59, no.5, pp.1319-1326, May 2011
10. Lashkarian, N.; Nassiri-Toussi, K.; Jula, P.; Kiaei, S.; , "Performance Bound on Ergodic Capacity of MIMO Beam-Forming in Indoor Multi-Path Channels," *Communications, IEEE Transactions on*, vol.58, no.11, pp.3254-3264, November 2010
11. Hyungseok Kim; Junghan Lee; Copani, T.; Bazarjani, S.; Kiaei, S.; Bakkaloglu, B.; , "Adaptive Blocker

Dr. Sayfe Kiaei
School of Electrical, Computer and Energy Engineering
Arizona State University, Tempe, AZ 85287

Rejection Continuous-Time $\Sigma\Delta$ ADC for Mobile WiMAX Applications," *Solid-State Circuits, IEEE Journal of* , vol.44, no.10, pp.2766-2779, Oct. 2009

12. Kitchen, J.N.; Chu, C.; Kiaei, S.; Bakkaloglu, B.; , "Combined Linear and Δ -Modulated Switch-Mode PA Supply Modulator for Polar Transmitters," *Solid-State Circuits, IEEE Journal of* , vol.44, no.2, pp.404-413, Feb. 2009
13. Sang-Soo Je; Rivas, F.; Diaz, R.E.; Jiuk Kwon; Jeonghwan Kim; Bakkaloglu, B.; Kiaei, S.; Junseok Chae; , "A Compact and Low-Cost MEMS Loudspeaker for Digital Hearing Aids," *Biomedical Circuits and Systems, IEEE Transactions on* , vol.3, no.5, pp.348-358, Oct. 2009
14. Taleie, S.M.; Copani, T.; Bakkaloglu, B.; Kiaei, S.; , "A Linear Digital IF to RF SD DAC Transmitter With Embedded Mixer," *Microwave Theory and Techniques, IEEE Transactions on* , vol.56, no.5, pp.1059-1068, May 2008
15. Wing-Yee Chu; Bakkaloglu, B.; Kiaei, S.; , "A 10 MHz Bandwidth, 2 mV Ripple PA Regulator for CDMA Transmitters," *Solid-State Circuits, IEEE Journal of* , vol.43, no.12, pp.2809-2819, Dec. 2008.
16. Lyles, U. J.; Copani, T.; Bakkaloglu, B.; Kiaei, S.; , "An Injection-Locked Frequency-Tracking $\Sigma\Delta$ Direct Digital Frequency Synthesizer," *Circuits and Systems II: Express Briefs, IEEE Transactions on* , vol.54, no.5, pp.402-406, May 2007
17. Khalil, W.; Bakkaloglu, B.; Kiaei, S.; , "A Self-Calibrated On-Chip Phase-Noise Measurement Circuit With -75 dBc Single-Tone Sensitivity at 100 kHz Offset," *Solid-State Circuits, IEEE Journal of* , vol.42, no.12, pp.2758-2765, Dec. 2007
18. Chen, X.; Kiaei, S.; , "Pulse generation scheme for low-power low-complexity impulse ultra-wideband," *Electronics Letters* , vol.43, no.1, pp.44-45, Jan. 4 2007
19. Carlosena, A.; Wing-Yee Chu; Bakkaloglu, B.; Kiaei, S.; , "Randomized Carrier PWM With Exponential Frequency Mapping," *Power Electronics, IEEE Transactions on* , vol.22, no.3, pp.960-966, May 2007
20. Abedinpour, S.; Bakkaloglu, B.; Kiaei, S.; , "A Multistage Interleaved Synchronous Buck Converter With Integrated Output Filter in 0.18 μm SiGe Process," *Power Electronics, IEEE Transactions on* , vol.22, no.6, pp.2164-2175, Nov. 2007
21. Kitchen, J. N.; Deligoz, I.; Kiaei, S.; Bakkaloglu, B.; , "Polar SiGe Class E and F Amplifiers Using Switch-Mode Supply Modulation," *Microwave Theory and Techniques, IEEE Transactions on* , vol.55, no.5, pp.845-856, May 2007
22. A Multistage Interleaved Synchronous Buck Converter With Integrated Output Filter in 0.18 micron. , S Abedinpour, B Bakkaloglu, S Kiaei - Power Electronics, IEEE Transactions on, Nov. 2007, Volume: 22, pp - 2164-2175
23. [Delta-sigma \(\$\Delta\Sigma\$ \) frequency synthesizers for wireless applications](#) - B Bakkaloglu, S Kiaei, B Chaudhuri - Computer Standards & Interfaces, 2007 – Elsevier, Analog Computer Standards & Interfaces Volume 29, Issue 1 , January 2007, Pages 19-30
24. Pulse generation scheme for low-power low-complexity impulse ultra-wideband, Chen, X.; Kiaei, S.; Electronics Letters; Volume: 43 Issue: 1 Jan. 2007 ; Page(s): 44-45
25. Bandwidth extension technique for polar modulated RF transmitters ; Bakkaloglu, B.; Kiaei, S.; Dwyer, R.; Electronics Letters; Volume: 42 Issue: 8 13 April 2006 ; Page(s): 476- 478 ;
26. Frequency modulated bandpass SD chirp synthesizer for sensor applications; Chung, H.H.; Lyles, U.; Copani, T.; Bakkaloglu, B.; Kiaei, S.; Electronics Letters; Volume: 42 Issue: 16 August 3, 2006 ; Page(s): 917- 918
27. Radiation Hardened by Design RF Circuits Implemented in 0.13 mm CMOS Technology; Chen, W.; Pouget, V.; Gentry, G. K.; Barnaby, H. J.; Vermeire, B.; Bakkaloglu, B.; Kiaei, K.; Holbert, K. E.; Fouillat, P. ; Nuclear Science, IEEE Transactions on ; Volume: 53 Issue: 6 Part=1, Dec. 2006 ; Page(s): 3449-3454 ;

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28. Analysis of Single Events Effects on Monolithic PLL Frequency Synthesizers ; Chung, H. H.; Chen, W.; Bakkaloglu, B.; Barnaby, H. J.; Vermeire, B.; Kiaei, S. ; Nuclear Science, IEEE Transactions on ; Volume: 53 Issue: 6 Part=1, Dec. 2006 ; Page(s): 3539-3543
29. Pulse generation scheme for low-power low-complexity impulse ultra-wideband
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89. "Communication and Signal processing Circuits for ADSL/VDSL system," international workshop on design of mixed-mode integrated circuits and applications, Guanajuato, Mexico, July 1998. [S. Kiaei]
90. "Analysis of Adaptive CMOS Down Conversion Mixers," Proceedings of the 8th Great Lakes Symposium on VLSI, Feb. 1998. [Sandalci, C.K.; Kiaei, S.]
91. "DC offset correction for direct conversion transceivers," Great Lake VLSI Symposium, Lafayette, Louisiana, 1998. [C. Sandalci, S. Kiaei]*
92. "Fundamentals of ADSL system," SuperComm, Atlanta, GA, June 1998. [S. Kiaei]
93. "Low-Power RF Design," Design Automation Conference (DAC), Anaheim, CA, June 1997. [S. Kiaei]
94. "Adaptive Multi-user Detector for Asynchronous DS-CDMA in Rayleigh Fading," Transactions on Circuits and Systems II: Analog and Digital Signal Processing, June 1997. [Dutta, A.K.; Kiaei, S.]
95. " Δ - Σ Frequency-to-Time Conversion by Triangularly Weighted ZC Counter," International Symposium on Low Power Electronics and Design, Aug. 1997. [Hovin, M.; Kiaei, S.; Lande, T.S.]
96. "Introduction to the Special Issue on Low Power Wireless Communications," IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing, June, 1997. [Kiaei, S.; Friedman, E.G.]
97. "Low Power Frequency-to-Time Conversion for Cellular Systems Using Predictive Zero-Crossing," 1997 IEEE 47th Vehicular Technology Conference, May 1997. [Dutta, A.K.; Kiaei, S.; Talwalkar, S.A.]
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102. "Predictive Zero-Crossing Frequency Discrimination for Cellular Systems, Part I and II." 47th Vehicular Technology Conference, VTC 97, Phoenix, AZ, May 97. [A. Dutta, S. Kiaei]
103. "CDMA Multi-user Cancellation," , Int. Conf. On Acoustics, Speech and Signal Processing, Munich, Germany, April 97. [A. Dutta, S. Kiaei]
104. "Digitally Correcting Schemes for Oversampled A/D," Int. Symp. On Circuits and systems, London, UK, 1994. [S. Abdenadher, S. Kiaei, G. Temes, R. Schreier]*
105. "Multi-Rate Transformation of Recurrence Equations," Int. Conf. on ASAP, Venice, Italy, Oct. 1993. [Li Aihua, Y. Zheng, S. Kiaei]

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106. "Adaptive Digital Correction for Dual Quantization Σ/Δ Modulators," IEEE International Symposium on Circuits and Systems, May 1993. [Kiaei, S.; Abdennadher, S.; Temes, G.C.; Yang, Y.]
107. "Analog Logic Techniques Steer Around the Noise," IEEE Circuits and Devices Magazine, Volume: 9, Issue: 5, Sept. 1993; Pages:18 – 21 [Allstot, D.J.; Kiaei, S.; Zele, R.H.]
108. "Folded Source-Coupled Logic vs. CMOS Static Logic for Low-Noise Mixed-Signal ICs," IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications, Sept. 1993. [Allstot, D.J.; San-Hwa Chee; Kiaei, S.; Shrivastawa, M.]
109. "Multi-Rate Transformation of Directional Affine Recurrence Equations," International Conference on Application-Specific Array Processors, Oct. 1993. [Zheng, Y.; Kiaei, S.]
110. "Adaptive self-correcting $\Sigma-\Delta$ modulators," International Conference on microelectronics, Tunisia, 1992. [S. Abdenadher, S. Kiaei, G. Temes]*
111. "Adaptive Self-Calibrating Delta-Sigma Modulators," Electronics Letters, Volume: 28, Issue: 14, 2 July 1992; Pages: 1288 – 1289. [Abdennadher, S.; Kiaei, S.; Temes, G.; Schreier, R.]
112. "Enhancement Source-Coupled Logic for Mixed-Mode VLSI Circuits," IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing, Volume: 39, Issue: 6, June 1992; Pages: 399 – 402. [Maleki, M.; Kiaei, S.]
113. "On-line Adaptive Digital Correction of Dual-Quantization Delta-Sigma Modulators," Electronics Letters, Volume: 28, Issue: 16, 30 July 1992; Pages: 1511 – 1513 [Yaohua Yang; Schreier, R.; Temes, G.C.; Kiaei, S.]
114. "Piecewise Linear Schedules For Recurrence Equations," Workshop on VLSI Signal Processing, Oct. 1992. [Rajopadhye, S.; Mui, L.; Kiaei, S.]
115. "Synthesis Techniques for CMOS Folded Source-Coupled Logic Circuits," IEEE Journal of Solid-State Circuits, Aug. 1992. [Maskai, S.R.; Kiaei, S.; Allstot, D.J.]
116. "A Folding Transformation for VLSI IIR Filter Array Design," Proc. of International Conference on Acoustics, Speech, and Signal Processing, Toronto, Canada, pp. 1237-1240, May 1991. [S. Rajopadhye, S. Kiaei]
117. "Systematic Derivation of Multi-Rate VLSI Arrays for the Solution of Toeplitz Matrices," IEEE Great Lakes Symposium on VLSI, March 1991. Proc. of IEEE Pacific Rim Conference on Communications, Computers, and Signal Processing, Victoria, BC, Canada, pp. 623-626, May 1991. [S. Kiaei]
118. "CMOS Source-Couple Logic for Mixed-Mode VLSI," Proc. of International Symposium on Circuits and Systems, New Orleans, Louisiana, pp. 1608-1611, May 1990. [S. Kiaei, S.H. Chee, D. Allstot]
119. "VLSI Design of Multi-Rate Arrays," Proc. of International Conference on Acoustics, Speech, and Signal Processing, New Mexico, pp. 1049-1052, 1990. [L. Aihua, S. Kiaei]
120. "Comparison of Low-Noise Current-Mode Logic Circuits for High Performance Mixed-Mode Applications," Proc. of International Symposium on Circuits and Systems, New Orleans, Louisiana, May 1990. [S. H. Chee, S. Chow, S.S. Lee, S. Kiaei, D. Allstot]
121. "VLSI Design of Dynamically Reconfigurable Array Processors-DRAP," Proc. of International Conference on Acoustics, Speech, and Signal Processing, Glasgow, Scotland, 1989. [S. Kiaei, J. Durgham]
122. "VLSI Design of Bit/Serial Adaptive IIR Filters," Proc. of IEEE Pacific Conference on Communications, Computers, and Signal Processing, Victoria, Canada, pp. 650-652, June 1989. [R. Badyal, S. Kiaei]

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123. "CCA Approach for ARMA Spectral Analysis," Proc. of IEEE International Symposium on Circuits and Systems, Portland, OR, pp. 1319-1322, May 1989. [S. Kiaei, L. Luo]
124. "Canonical Correlation Analysis (CCA) for ARMA Spectral Estimation," IEEE International Symposium on Circuits and Systems, May, 1989. [Kiaei, S.; Luo, L.]
125. "VLSI Implementation of Adaptive Bit/Serial IIR Filters," IEEE Pacific Rim Conference on Communications, Computers and Signal Processing, June 1989. [Badyal, R.; Kiaei, S.]
126. "VLSI design of WAP for Recursive Equations," VLSI Signal Processing, 1988. [S. Kiaei, U. Desai]
127. "Independent Data Flow Wavefront Array Processors for Recursive Equations," Proc. of 20th Annual Conference on Information Sciences and Systems, Princeton University, NJ, 1986. [S. Kiaei, U. Desai]
128. "A Stochastic Realization Approach to Reduced-Order Hierarchical Estimation," Proc. of 24th IEEE Conference on Dec., Ft. Lauderdale, FL, pp. 416-421, December 1985. [U. Desai, S. Kiaei]
129. "Hierarchical Estimation Algorithms," Proc. of IEEE Conference on Man, Cybernetics, and Systems, Tucson, AZ, October 1985. [U. Desai S. Kiaei]
130. "Approximation of Markovian Models with Non-Constant Parameters," Proc. of 23rd IEEE Conference on Dec., Las Vegas, NV, pp. 1642-1644, December 1984. [U. Desai, S. Banerjee, S. Kiaei]
131. "A Canonical Correlation Approach to Reduced-Order LQR Design," Proc. of 23rd IEEE Conference on Dec., Las Vegas, NV, pp. 1523-1528, December 1984. [U. Desai, S. Banerjee, S. Kiaei]

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GRADUATE STUDENT ADVISEES & RESEARCH PROJECT

(Partial list of Students graduated, current employment to the best of my knowledge)

1. J. Durgam, VLSI Design of Dynamically Reconfigurable Array Processors, MSEE, 1988. Intel.
2. J. Gilbert, Minimization Techniques for PLAs, MSEE, 1988, Tektronix Inc.
3. L. Luo, CCA Methods for ARMA Spectral Estimation, MSEE, 1989. Berkeley Research Center
4. E. Zahl, Enhancement Methods for A/D Noise Reduction, MSEE, 1989. AT&T
5. L. Aihua, Synthesis of MRAs, MSEE, 1990. Intel.
6. F. Aslam, Image Restoration Methods, MSEE, 1990.
7. S.H. Chee, FSCL Circuits for Mixed-Mode IC's, MSEE, 1990. Linear Tech.
8. C. Dawson, MSEE, 1990. Boeing
9. A. Chow, Source-Coupled Logic ALU, MSEE, 1990. Intel
10. S. Maskai, Decimation Filters Using FSCL Circuits, MSEE, 1991. Intel
11. L. Louis, VLSI Implementation of Toeplitz Matrices, MSEE, 1991.
12. R. Badyal, Bit/Serial VLSI Design of IIR Filters, MSEE, 1992, HP
13. Lap Mui, Piece-Wise Linear Schedule for VLSI Arrays, MSEE, 1992. HP
14. S. Abdennadher, Adaptive Sigma-Delta Modulators, MSEE, 1992. Level One / Intel.
15. H. Bribech, Second Order Adaptive A/D Schemes, MSEE, 1992.
16. B. Hickman, MSEE, 92. Tektronix
17. M. Maleki, Current-Mode Flash A/D, MSEE, 1992. University of Oregon
18. Man Wong, Low-Noise Decimation Filter for Mixed-Mode ICs, MSEE, 1993, Motorola.
19. Anu Krishna Swamy, Low Noise IC Blocks for Mixed-mode IC's, MSEE, 1993, Ph.D., 1997.
20. Manu Srivastava, Comparison of Differential Logic (FSCL, CVSL, DSLL), MSEE, 1994, Intel.
21. Joel Oren, VLSI Design of Asynchronous FIR Filters, MSEE thesis, Feb. 1994. E-Systems.
22. Y. Zheng, VLSI Design and Synthesis of Multi-Rate Arrays, Ph.D. March 94, Hughes Research.
23. Satish Kulkarni, Low-Sensitivity Filters, MSEE, 1995, Motorola.
24. Amit Dutta, Multi-user Interference Cancellation, Ph.D, Dec. 97, Faculty, India.
25. Dwight Poplin, Multiplierless MPEG Decoder, MSEE, 1996. HP.
26. Maxim Scarpa, Adaptive I/Q Miss-match Correction for Direct Conversion Receivers, MSEE 1998.
27. Jeff McNeal, Sigma-Delta Frequency-to-Time Conversion, MSEE, 1998. Level One Comm.
28. Julia Vogel, Adaptive DC offset Cancellation, MSEE, 1998. Faculty in Germany.
29. Takao Inoue, MS, Echo Cancellation for ADSL, 1998. MSEE, The U of Texas at Austin.
30. Navid Lashkarian, Frequency off-set estimation and Synchronization of OFDM systems, Ph.D., June 1999. Broadcom Inc. & Faculty at UC San Jose.

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31. Guner Arslan, (co-advisor with B. Evans), "Fast Equalization for DMT systems, with applications to ADSL," Ph.D. The University of Texas at Austin, 2000
32. Salem Abdennadher, I/Q Mismatch Correction for RF Wireless transceivers, Ph.D., Level One Comm/Intel.
33. Can Sandalci, DSL Line Driver, Ph.D., 2001, Intel.
34. Dean Badillo, Low-Cost VCO Ring Oscillators, PhD, 2004, Intel, Chandler,
35. Siamak Abedinpour, PhD, 2005 Freescale, Tempe, Arizona
36. Hemanth Shivalingaiah, Multi-Band Low Noise Amplifiers, Ph.D., 2006, Intel,
37. Shahin Farahani, PhD, 2006, Qualcomm Inc,
38. Nazanin Darbanian, M.S. Freescale, Tempe, Arizona
39. *Joe Rutkowski, Joseph, MS, 2004, Phillips.*
40. *Chaudhuri, Bikram, Synthesizer, MS/PhD, MS 2004.*
41. *Zhang, Jiandong, MEMs, MEMS, December-04*
42. *Afsahi, Ali, MS/PHD, UC San Diego, QUALCOMM, Connection One*
43. *Chen, Xiaomin, UWB, PHD, 2007, SRC/Motorola*
44. *Jali, Hilda, Power Management, MS, June-05,*
45. *Xuejin Wang, RF Optimization, 2006 CAD tools, PhD, Neo-Linear*
46. *Umar Lyles, Power Amplifier, MS, 2006. Texas Instruments*
47. MS, Erika Munoz, RADHARD, 2007, Intel
48. Waleed Khali, (Co-Advisor), Professor at Ohio State
49. Jennifer Kitchen, PhD, 2009, Professor at ASU
50. Shahin Mehdizad Taleie, RFDAC, PhD, 2009, Qualcomm
51. Ilker Deligoz, PHD, 2009, Qualcomm
52. Hyung Kim, PhD, Jan 2010, Intel
53. Jung Le, PhD 2010, Intel, TI
54. Syed Naqvi, PhD, 2012, Intel.
55. Todd Martin, MS, 2011, TI
56. Seungkee Min, PhD, 2011, Intel
57. Ali Meamar, Post Doc, RFIC 2013
58. Hitesh Khunti, MS 2013, Qualcom
59. Debashis Mandal, Post Doc, 2018
60. Edgar Martinez, PhD, 2015, Qualcomm
61. Chirag Desai, MS, 2016, Qualcom
62. Sanjay Avasarala, MS, 2016
63. Amir Ayati, PhD Expected 2017

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64. Pasisa Mahmoudi, PhD, Expected 2017
65. Li Ming, MS, 2017
66. Qirong Peng, MS, 2017
67. Yu Geng, PhD, 2018
68. Chai Yong, MS: 2015, PHD: 2019, IDC
69. John Sochaki, PhD, 2019, ViaSat Comm.,
70. Shrikant Singh, MS: 2016, TI, PhD, 2019

UNIVERSITY COMMITTEES

Various Committees at ASU, Oregon State University, etc.

INDUSTRY COMMITTEES

Arizona Telecommunications and Information Council (ATIC), Board Member

CAS Fellows Committee (ends December 31, 2006)

- *IEEE CAS Phoenix Chapter Organizers (the committee is in the process of determining new chair – current chair not active)*
- *Executive Committee, RFIC 2006.*
- *Technical Program Comm, IEEE RFIC 2006.*
- *Executive Committee, Conferences, International Solid State System's Conference.*
- *IEEE CAS Society, VLSI Technical Comm. Member*
- *Editorial Board, IEEE Communications Surveys & Tutorials*
- *Radio Frequency Integrated Circuits- RFIC 2006*
- *IEEE RF Integrated Circuits Conference, Committee Chair for two workshops*
- *International Microwave Symposium, IMS-MTT 2006*
- *Int. Symposium on Circuits and Systems - ISCAS 2006*
- *Wireless Networks & Emerging Technologies, WNET06*
- *Midwest Symposium on Circuits and System*
- *Arizona Governor IT Advisory Committee – GITA*
- *Arizona Telecom – ATIC*

INSTRUCTIONAL SUMMARY

- Digital IC Design, Analog IC Design, Advance CMOS Analog IC, VLSI, RFIC Design
- Wireless Transceiver Design, Wireless Communications, GPS, Telecomm Systems, Digital Communication
- Signal Processing, Advance DSP, Communication, Digital Communication, Digital Audio Processing,
- Computer Architecture, Microprocessor System Architecture, Pipeline Array Processing