School of Electrical, Computer and Energy Engineering Arizona State University, Tempe, AZ 85287

Sayfe@asu.edu

Sayfe Kiaei

Professor, Motorola Endowed Chair Professor School of Electrical, Computer and Energy Engineering, Arizona State University, Tempe, AZ

FIELDS OF SPECIALIZATION

- Analog, Digital, VLSI, Processor, ASIC, RF Integrated Circuits
- Power Management IC, Battery Management, Energy System, Energy Management
- Signal Processing, Digital Signal Processing, Adaptive Signal Processing, Video & Audio Signal Processing
- Sensors, Bio-electronics, Bio-sensors, Hearing Aid Electronics, Implanted devices electronics
- Communication Systems, Wireless Communications, Wireline Communication System
- Adaptive Audio Array processing, Audio and Acoustic & Speech processing,

DEGREES

- **Ph.D.**, Electrical and Computer Engineering, Washington State University, 1987
- M.S., Electrical and Computer Engineering, Washington State University, 1984
- B.S.E.E., Electrical Engineering, Northeastern University/WSU, 1982

ACADEMIC POSITIONS

Fall 2001-Present: Professor, Motorola Endowed Chair Professor in Analog and RFIC School of Electrical, Computer and Energy Engineering, Arizona State University, Tempe, AZ

- Professor: Research and teaching in integrated circuits, RF circuits and systems, Communications, Wireless and Wireline transceiver, mixed-signal and Analog IC, Sensors, Power management IC, Signal processing, Bio-electronics
- Research Projects:
 - o Analog and digital IC, Radio Frequency IC, RF transceiver
 - o VLSI, Processor System Architecture, ASIC
 - o Power Management IC, Battery Management & Sensing, Integrated Power Electronics
 - o Digital Signal Processing, Audio processing, adaptive signal processing, Array processing, AI
 - Wireless communication system, wireless modems, 1G, 2G GSM, 3G CDMA, 4G LTE, 5G wireless mobile system, LTE, WiFi, Bluetooth, Wireless system standards
 - Wireline Communication system and transceivers, MODEM standards, CABLE MODEM DOCIS, DSL
 - o Signal Processing, Digital Signal Processing, Adaptive Signal Processing
 - o Adaptive Audio Array processing, Audio and Acoustic & Speech processing,
 - Sensors, Bio-electronics, Bio-sensors, Hearing Aid Electronics, Implanted devices electronics
 - Research Funded by NSF, USAID, DARPA, JPL, NASA, Motorola Inc., Intel Inc., Broadcom, Qualcomm, Raytheon, General Dynamics, Texas Instruments, and over 10 other industries. List of Current significant research awards:

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- Partnership Center for Energy systems, USAID, 2015-2020, \$18M. Principle Investigator
- o QESST NSF ERC Center on Solar Energy, Battery Management, PMIC, NSF, 2010-2020, \$36M, Co-PI, Test-bed Director
- Solar Energy Development in ME, Private funds and World Bank, \$2M
- Connection One NSF Center, Director, 2004-Present, Total funding \$10M, average annual funding over \$750K.

2004-Present, Director and founder of NSF IUCRC Center Connection One, School of Electrical, Computer, and Energy Engineering, Arizona State University, Tempe, AZ; https://connectionone.org

The NSF Connection One Industry/University Cooperative Research Center was established the center in 2002 with focus on communication system, integrated Circuits and Systems, wireless system, RF, sensors, and related areas. The center has five university member with over 30 industrial members. Total funding over \$10M, annually over \$500K. www.connectionone.org

2014-2020, Director, USAID, US-PCASE: Center for Advance Studies in Energy, Funding \$18M. https://uspcase.asu.edu/

- **Director and PI:** PCASE Partnership Center for Energy systems, Energy Center funded by the USAID.
- USIAD Centers for Advanced Studies in Energy program (USPCAS-E) is a partnership between Arizona State University and two leading Pakistani universities: the National University of Science and Technology (NUST) Islamabad and the University of Engineering and Technology in Peshawar (UET).
- PCASE has developed two new Graduate schools of Energy. Within 5 years, the center has over 1000 MS and PHD Students, with 14 new energy degrees in MS and PhD, two new building with 20+ energy labs in the power system, grid, power electronics, renewable energy, PV, Wind, Hydro, bio-fuel, fuel cell, batteries and storage, and thermal areas.

2008-2012: Associate Dean of Research, Ira A. Fulton Schools of Engineering, Arizona State University

Responsible for leading the research infrastructure, promoting and developing research programs with industry and federal agencies, leading large multi-university proposals, investing and providing seed funding to foster new research areas, and promoting graduate program in the college of engineering. Research Enterprise support included:

- Increase College of Engineering research funding from \$50M to over \$80M.
- Working with Vice President for Research, Dean's, and directors on University-wide research initiatives.
- Established the first NSF Engineering Research Center (ERC) at the ASU on Solar Energy QESST. Managed, organized and planned the ERC proposal process. ASU is the lead school partnering with MIT, Georgia Tech, U of Delaware, Cal-Tech, U of New Mexico, and UA.
- Lead several trans-disciplinary 4M research projects (4M: multi-million, multi-investigator, multidisciplinary, multi-university grants) in energy, security, and related initiatives.
- Oversight of over 20 existing research centers in the college of Engineering.
- Engage with industry and federal government to establish new research collaborations.
- Organized workshops and supported proposals for NSF, NIH, DOE, DOD, DARPA, etc.
- Organized workshops for new assistant professors to apply for NSF CAREER Awards. ASU CAREER awards grew from 3 annual awards in 2008 to over 15 CAREER awards by 2012.

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- Research Administration and pre-award proposal administration for the schools. Developed a decentralized research administration and advancement team for the Schools supporting 5 schools, 12 departments, over 220 engineering faculty, with funding over \$70M.
- Annual budget over \$7M for supporting research centers, seed funding for new center, cost sharing, proposal support, equipment and infrastructure support, graduate scholarships, and research administration.
- ADR Staffs included, Director of industrial and government liaison, Director of research administration, and 14 research advancement staff.
- Graduate Programs: Recruiting, Fellowships, marketing, outreach, coordination with departments

1997-2001, Adjunct Professor, Electrical and Computer Engineering Dept., The University of Texas, Austin, Texas, Taught graduate courses at UT Austin on Introduction to Telecommunication System and Digital Communications. Co-advised two Ph.D. program committees in IC design and Telecomm (while at Motorola)

1987-1993, NSF Center For Digital / Analog IC (CDADIC) Co-Director, NSF IUCRC Center director at Oregon State University. The CDADIC was established the center in 1987 with focus on integrated circuits at WSU, UW, and OSU with over 20 industrial members - https://cdadic.oregonstate.edu/

1987-1993, Assistant / Associate Professor (Tenured) Electrical and Computer Engineering Department, Oregon State University, Corvallis, OR

- Research and classes in Electronics, DSP, Communication system and networks, Wireless systems, MODEMS, Graduated 30 MS and Ph.D. students.
- Faculty Chair, Computer Engineering Program, Developed a new Computer Engineering Program at OSU in 1987

INDUSTRIAL POSITIONS

1993-2001: Motorola Inc., Senior Member of Technical Staff, Personal Communication Sector, Austin, Texas - Worked projects related to wireless communications, two way radios, wireless networks, ADSL and MODEM, RF, and related areas.

- Motorola Cellular Division, Wireless Technology Center (WITC), 1997-2002. Responsible for development of integrated circuits and systems for wireless handset. Lead number of projects including cellular (2G, 3G, 4G), wireless connectivity (Bluetooth and WIFI transceiver), GPS and location Receiver, wireless networks, 2-way radios and related areas. Worked on the development of various subcomponents including system design, link budget, RF front-end, filtering, analog front-end, power management, battery management, and baseband circuits and systems.
- Motorola Semi-conductor products sector (SPS), Broadband Products Operations, 1995-1997, Worked on the development of XDSL (ADSL, VDSL, G.lite) systems including OFDM, modulation, synchronization, equalization and the development of a single chip ADSL transceiver (*CopperGold*Tm). The transceiver contained Analog Front End (A/D, D/A, Hybrid), DMT, modulation/demodulation, FFT, IFFT, echo canceler, time domain equalizer, front-end constellation mapping, Trellis code modulation, Viterbi decoder) and an on-chip DSP core.

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- Land Mobile Products Sector LMPS 1993-1995, Responsible for Wireless digital two-way radios, hot
 spot wireless network, next generation of digital two-way radios, "<u>Talk about Radios</u>", Japanese cellular
 systems (PHS).
- Standards, Represented Motorola in various standards including 2G-4G, GPS, Bluetooth working group, WiFi, 802.11, and DSL standards including T1E1, International Telecommunication Unit (ITU), T1E1, ETSI, 3GPPP, Universal ADSL Working Group (UAWG), Bluetooth working group, G.Lite working group, etc.
- University relations, Responsible for the development of collaborative research programs with several
 universities. Responsible for funding research in the areas of Wireless Transceiver IC Design, RF, and
 mixed-signal and baseband system architecture.

1985-87: Member of Research Staff, Boeing Co., Bellevue, Wa, Flight Systems Research and Technology Center, summer. Design Engineer, Hardware and CAD tool development for system control.

AWARDS

- IEEE Fellow 2004-Present
- IEEE Fellows CAS Committee Chair, 2009-2012
- Global Standards Award, For contributions in the International Telecommunication Unit (ITU) for Asymmetric Digital Subscriber Line (ADSL) G.Lite Standards. Motorola Inc., 1999.
- 10X Cycle Reduction Award, for development of new IC design process from DSP algorithm to IC layout, Motorola Inc., 1995.
- IEEE Darlington best paper Award, IEEE Circuits and Systems Society Best Paper Award, 1995. For "Characterization and Comparison of CMOS FSCL Circuits with Conventional CMOS for mixed-signal ICs," Published at: IEEE Trans. on Circuits and Systems II, Sept. 93.
- Carter Best Teaching Award, College of Engineering Best Teacher Award, Oregon State University, 1992. For "outstanding and inspirational teaching in the College of Engineering". Award is selected by the confidential vote of all of the undergraduate students in the College of Engineering among over 125 professors in the College.
- Industrial University Fellowship (IUF) Award, National Science Foundation, 1993.
- Research Initiation Award, National Science Foundation, 1990-93.
- Outstanding Graduate Student Scholarship, Azur-Data Inc. WSU, 1984

RESEARCH PROJECTS

Partial list of Research Awards:

- USAID, PCASE Center for Energy systems, 2015-2020, \$18M. PI and Director
- NSF, QESST NSF ERC Center on Solar Energy, 2010-2020, \$36M, Kiaei, Co-PI, Testbed Director,
- Private Donors, \$1.5M, 2012-2015, Solar Energy Development

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- NSF IUCRC Center, Connection One 2002-present, Over \$10M as PI, over \$0.5M annual center awards
- NSF, Micro-Power Multi-Phase MEMS Hearing Aid, 2007-2011, \$500K
- NSF Design for Implantable Bio-Sensors, 2007-2009, \$480K
- Science Foundation of AZ, PEPER- Photovoltaic Environmental Performance and Reliability for the Arizona-Wide Electric Grid, 2009-2013, \$1.2M
- SRC –Self Characterization for Calibration and Process Feedback of MEMS Devices, 2011-2014, \$300K
- NSF- Cognitive MIMO Communications for Dynamic-Spectrum Wireless Networks 2012-2014, \$150K NSF, Autonomous Self-Healing Sensor Network Radio, 2010-2014, \$250K
- DARPA, Neural-Enabled Prostheses with Sensorimotor Integration, \$500K
- NSF, Microwave Sensors for Vital Signs Monitoring Device Design, 2011-2013, \$250K
- NSF, Various REU funds, 8/31/12-8/31/13, \$400K
- DARPA, Nano-Mechanical RF Band pass resonator for 2GhZ RF Applications, with JPL, \$2.2 M, 2002-2005,
- Qualcomm, Connection One Center, Various projects in 3G-5G, WiFi (802.11), GPS, and Bluetooth, 2005-Present, \$1.2M
- Texas Instruments, Various projects in Battery & Power management, and RFIC, 2005-20012, \$1.5M
- Motorola Inc., Various projects in Battery & Power management, and RFIC, 2002-2010, \$1.2M.
- SIRF Technologies, GPS Transceiver, 2005, \$300K.
- Ridgetop Inc., RF Harsh Environment, \$200K
- Freescale Semiconductor, PWM, Battery & Power management, 2006, \$150K
- State of Arizona, WINTECH- Wireless Integrated Nano Technology Center Support (2005-2009), Ranging from 450K annually from 2005-2009.
- BAE Systems; "New Techniques for Time Measurement Circuits LiDAR; 2005-2008; \$650K
- SRC (Semi-conductors research Corp), Ultra-Wideband Transceivers for cellular and WiFi 802.11, \$225K, 2001-2003
- Intel Corporation, Design of Multi-Standard RF Front-End Circuits for Cellular and WiFi, \$300K, 2002-2005
- National Science Foundation, Adaptive Compensation of Analog circuits imperfections using DSP methods, \$150K, 1996 (tie project with UC San Diego NSF center), 2010-2011
- Center for the Design of Analog/Digital IC's (CDADIC) 1987-1995, At Oregon State, \$1.5M
- Low Power IF processing for Direct Digital Transceivers, *Motorola Inc*, \$100K, 93.
- Hewlett-Packard Faculty Chair position in Mixed-Signal IC, HP, 1995-97, \$500K
- National Science Foundation, Motorola Inc. Faculty Industry Fellowship, \$250K, 93-94.
- National Science Foundation, Research Initiation Award (RIA) (same as current CAREER Award),
 Synthesis and Automatic Derivation of Multi-Rate VLSI Arrays for DSP Algorithms, , 90-93. \$320K.
- CDADIC, various projects on Low-Noise Source Coupled Logic (SCL), Mixed-Mode IC's, CDACIC \$350K, 1988-1992.

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- Decimation Filters for A/D Noise Enhancements, Tektronix, Inc., \$100K, 1988.
- Various grants for IC Fabrication (DARPA/MOSIS, VLSI), testing equipment (Tek, HP), DSP system development (TI, Motorola), ranging in various amounts up to \$200K/year. At Oregon State, 1988-1997.

PROFESSIONAL RECOGNITION

- IEEE Fellow, 2004-Present
- IEEE Fellow Committee Chair, CAS, 2008-2010
- IEEE Fellow Committee member, 2007-2010.
- IEEE Senior Member, 1993-Present, IEEE Member 1987-1992.
- IEEE Faculty Advisor, Oregon State University, 1987-1990

IEEE Editorials

- IEEE Microwave Magazine, Editor,
- IEEE System Journal, Associate Editor, 2010-2011.
- IEEE Transactions on VLSI, Associate Editor, Jan 2001-2008.
- IEEE Communication Magazine, Editor, Feature Issues on "Circuits for Wireless and Wireline Communications," April 1999.
- IEEE Transactions on Microwave Theory and Techniques, editor, Special Issue on: "Radio Frequency IC Design," Dec. 1998.
- IEEE Transactions on Circuits and Systems-II, editor, Special Issue on: "Low-Power Wireless Communication Systems," June 1997.
- Associate Editor, IEEE Transactions on Circuits and Systems-II, 1993-1996.
- Editor and Reviewer for many IEEE journals and conferences
- Founding member of IEEE RF Integrated Circuits Symposium
- Associate Editor, IEEE Communications, Tutorial & Surveys Magazine, 2006-2009.

Conference Organizations

- RFIC Executive Committee members, 2000-2017
- RFIC Steering Committee Member, RFIC symposium, 1996-2017.
- RFIC Founding member, 1995-96.
- Technical Program Chair, IEEE International Sym. on Circuits and Systems, Phoenix, AZ, 2002.
- ISSCC Admin Council, Conferences Committee 2000-2005.
- General Chair, Radio Frequency IC (RFIC) Symposium, Seattle, WA, 2002.
- Technical Program Chair, RFIC Symposium, Phoenix, AZ, 2001.
- Finance Chair, RFIC symposium, Boston, MA, 2000.

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- Publicity Chair, RFIC symposium, Los Angeles, CA, 1999.
- Transactions Chair, RFIC symposium, Baltimore, MD, 1998.
- General Chair, Int. Sym. on Low-Power Electronics and Design (ISLPED), Monterey, CA, 97.
- Executive Committee Member, Int. Symp. On Low-Power Electronics and Design, 96-2000.
- Technical Program Committee Member of the following conferences:
 - International Conference on Circuits and Systems: 1996, 2000, 2001, 2004-2008
 - RFIC Symposium, 1996-2018
 - Application Specific Array Processing (ASAP): 2000-2002
 - Technical Program Chair, Int. Sym. on Low-Power Electronics and Design, Monterey, CA, 96.
 - Arizona Telecom Comm (ATIC)
 - GLS VLSI 1998, Lafayette, Louisiana, 1998
 - VLSI Design 98, Chennai, India, Jan. 1998.
 - ICECS, Lisbon, Portugal, 98.
 - Application Specific Array Processing, 1995-97, 2000
 - Vehicular Technology Conference, 1995-97.
 - Inter. Conf. on Intelligent Information Systems, D.C., 1994-95.
 - IEEE Pacific Rim Conference on Communications & Computers, Victoria, BC, Canada, 1991.

Invited talks, Panelist, Session Chairs, Workshop Speaker

Conference chair, Technical Program committee chair and TPC member, tutorials, workshops, session chair, etc. in RFIC, ISSCC, ISCAS, VLSI, ICASSP, Low-Power Symposium, ICC, Application Specific IC's, IMS, MTT, etc.

CONSULTANT

- Intel Inc. Chandler, AZ, 2002-2006: Development of 3G-4G Wireless transceiver.
- Sony Inc., San Diego, CA and Tokyo, Japan, 2002-2004: Review and development of various telecom cellular system architecture including 3G system architecture, and GPS system.
- Motorola Inc. 2002-2005: Supporting development of BT, WiFi, E911, GPS integrated circuits and systems for the cellular and mobile handsets.
- Hewlett Packard, Corvallis, OR 1990-1993: Various project on development of custom analog and digital IC's for printer and inkjet system. Some of this work was under consultation, and some under various research grants with Oregon State University.
- Tektronix Inc, Beaverton, OR 1988-1990: Design and Implementation of Data acquisition system for Spectrum analyzer, development of custom DSP algorithm for the Tektronix spectrum analyzer including system architecture, simulation, analysis, and design of oversampled data acquisition system.
- Boeing Commercial Aircraft, BCAC, Renton, WA 1985-1987: Development of Airplane Controller Model, Simulation and Implementation of Flight control, Model reduction, and system control.

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EXPERT WITNESS (Patent, IP)

Patent litigation, patent validity, IPR, expert reports, deposition, testimony, and trade secrets in the following areas (Complete list of cases available):

- Analog and Digital IC
- Radio Frequency Integrated Circuits
- Power Management, Battery Management, PMIC
- Wireless communication, 3G, 4G, OFDM, WiFi, 802.11, Bluetooth, and related areas
- Audio and acoustic signal processing, Audio Array processing
- Communication networks, Communication system
- Signal Processing, adaptive signal processing
- DSL, xDSL, VDSL, OFDM, Multi-Tone, and related areas
- Cable MODEM DOCIS MODEM, and related areas.
- Hearing AID
- Bio-Electronics, Heart monitoring system, Bi-sensors
- Satellite communications, Satellite Transceiver, ECHO and Multi-path cancelation circuits
- Wireline Communications, MODEM, Digital Subscriber Line, ADSL, VDSL, MODEM
- Wireless LAN, Wi-Fi, 802.11
- Bluetooth
- ZIGBEE
- GPS system, GPS receiver
- MEMS, Bulk Acoustic Wave Filters, SAW, MEMS resonators, MEMS accelerometer
- Wireless Standards (ITU, ETSI, 3GPPP, LTE) including AMPS, GSM, CDMA, WCDMA, LTE, 1G, 2G, 3G, 4G, BT, WiFi (802.11)
- Wireline standards including DSL, MODEM and DOCIS, and related standards ITU/ETSI

PATENTS, PUBLICATIONS

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Patents and Patent Applications

		inventor/au	priority	filing/creati	publication
Patent Number	title	thor	date	on date	date
		Timothy W.			
US-10653337-B2	Local object detection system	Markison,	8/18/16	8/18/17	5/19/20
		Siamak			
US-7372333-B2	Monolithic supply-modulated RF power amplifier and DC-DC power converter IC	Abedinpour,	2/3/03	2/3/04	5/13/08
		Thomas M.			
US-6661371-B2	Oscillator frequency correction in GPS signal acquisition	King,	4/30/02	4/30/02	12/9/03
		Siamak			
US-7218085-B2	Integrated ZVS synchronous buck DC-DC converter with adaptive control	Abedinpour,	5/24/02	5/27/03	5/15/07
		Bertan			
US-7528754-B1	Finite impulse response digital to analog converter	Bakkaloglu,	2/9/06	2/8/07	5/5/09
US-10791965-B2	Method and apparatus for wirelessly monitoring repetitive bodily movements	Sayfe Kiaei	10/19/15	4/12/19	10/6/20
		Shahin			
US-2007033000-A1	Efficient non-iterative frequency domain method and system for nonlinear analysis	Farahani,	7/19/05	7/19/06	2/8/07
	Compressed vector-based spectral analysis method and system for nonlinear rf	Shahin			
US-2006052988-A1	blocks	Farahani,	11/21/02	11/21/03	3/9/06
		Parisa			
US-2020266708-A1	Electronic circuit and method of controlling three-level switching converters	Mahmoudid	2/14/19	2/14/20	8/20/20

Standards Contributions

- 1. "Spectral Compatibility of ADSL: Frequency Overlap vs. FDM," T1E1, Dec. 97.
- 2. "Echo Cancellation for G.Lite Universal ADSL," OFDM, Universal ADSL Working Group, Atlanta, GA, Jan 98.
- 3. "8-bit QAM Constellation effects on reach for universal ADSL," OFDM, Universal ADAL Working Group, Atlanta, GA, Jan 98.
- 4. "Trellis Code Modulation coding gain for OFDM," Universal ADSL Working Group, Atlanta, GA, Jan 98.
- 5. "Monte Carlo Modeling and simulation of twisted pair wiring for OFDM," Universal ADAL Working Group, Atlanta, GA, Jan 98.
- 6. "Overlap Upstream/Downstream spectral allocation for OFDM ADSL," International Telecommunication Unit, Chicago, March 98.
- 7. "Echo Cancellation for ADSL OFDM," International Telecommunication Unit, Antwerp, Belgium, 98.
- 8. "Performance of Echo Cancellation ADSL in OFDM system in the presence of Near End Cross Talk (NEXT)," International Telecommunication Unit, Honolulu, Hawaii, June 98.
- 9. Presentations and editorials at various XDSL and OFDM standards: ITU, ETSI, UAWG, and T1E1, 97-99.
- 10. Presentations and editorials at various 3G and 4G and wireless standards including ITU, 3GPPP, 802.11, BT.

Books

"Design, Modeling and Testing of Data Converters, P Carbone, S Kiaei," F Xu - 2014 – Springer, © Springer-Verlag Berlin Heidelberg 2014

Refereed Journal Papers

1. CMOS Full-Duplex Mixer-First Receiver With Adaptive Self-Interference Cancellation S.-A. Ayati; A. Alizadeh; S. Kiaei, IEEE Transactions on Circuits and Systems I, Jan 2021.

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- 2. A 10-W X-Ban Class-F High-Power Amplifier in a 0.25m GaAs pHEMT Technology, A. Alizadeh; M. Yaghoobi; M. Meghdadi; A. Medi; S. Kiaei, IEEE Transactions on Microwave Theory and Techniques, Jan 2021.
- 3. An X-Band Class-J Power Amplifier With Active Load Modulation to Boost Drain Efficiency A. Alizadeh; S. Hassanzadehyamchi; A. Medi; S. Kiaei, IEEE Transactions on Circuits and Systems I: Sep 2020
- 4. In-Field Recovery of RF Circuits from Wearout Based Performance Degradation D. Chang; J. N. Kitchen; S. Kiaei; S. Ozev, IEEE Transactions on Emerging Topics in Computing, Jun 2020
- 5. A 50-V Isolation, 100-MHz, 50-mW Single-Chip Junction Isolated DC-DC Converter With Self-Tuned Maximum Power Transfer Frequency, C. Liu; D. Mandal; Z. Yao; M. Sun; J. Todsen; B. Johnson; S. Kiaei; B. Bakkaloglu, IEEE Transactions on Circuits and Systems II: Express Brief, May 2019
- 6. Wideband Hybrid Envelope Tracking Modulator With Hysteretic-Controlled Three-Level Switching Converter and Slew-Rate Enhanced Linear Amplifier, P. Mahmoudidaryan; D. Mandal; B. Bakkaloglu; S. Kiaei, IEEE Journal of Solid-State Circuits, 2019.
- 7. Low-Power/Low-Voltage Integrated CMOS Sense Resistor-Free Analog Power/Current Sensor Compatible With High-Voltage Switching DC-DC Converter, S. Singh; D. Mandal; B. Bakkaloglu; S. Kiaei IEEE Transactions on Circuits and Systems I, 2019
- 8. Adaptively Biased Output Cap-Less NMOS LDO With 19 ns Settling Time, D. Mandal; C. Desai; B. Bakkaloglu; S. Kiaei, IEEE Transactions on Circuits and Systems II: Express Briefs, 2019
- 9. Chirag Desai; Debashis Mandal; Bertan Bakkaloglu; Sayfe Kiaei, "A 1.66 mV FOM Output Cap-Less LDO With Current-Reused Dynamic Biasing and 20 ns Settling Time," IEEE Solid-State Circuits Letters Year: 2018, Volume: 1, Issue: 2, Pages: 50-53
- 10. Debashis Mandal; Chirag Desai; Bertan Bakkaloglu; Sayfe Kiaei, Adaptively Biased Output Cap-Less NMOS LDO with 19 ns Settling-Time;; IEEE Transactions on Circuits and Systems II: Feb 2019
- 11. Ayati, Mandal, Bakkaloglu, Kiaei, "Integrated Quasi-Circulator With RF Leakage Cancellation for Full-Duplex Wireless Transceivers,", IEEE Trans of Microwave theory and techniques, Dec 2017.
- 12. "A 50-mA 99.2% Peak Current Efficiency, 250-ns Settling Time Digital Low-Dropout Regulator With Transient Enhanced PI Controller", ChaiYong Lim; Debashis Mandal; Bertan Bakkaloglu; Sayfe Kiaei; IEEE Transactions on Very Large Scale Integration (VLSI) Systems; Year: 2017, Volume: 25, Issue: 8; Pages: 2360 2370
- 13. Doohwang Chang; Jennifer N. Kitchen; Sayfe Kiaei; "Sule Ozev, In-field Recovery of RF Circuits from Wearout Based Performance Degradation", IEEE Transactions on Emerging Topics in Computing, 2017.
- 14. Edgar Martí-Arbona; Debashis Mandal; Bertan Bakkaloglu; Sayfe Kiaei, A High-Voltage-Compliant Current-to-Digital Sensor for DC–DC Converters in Standard CMOS Technology, IEEE Transactions on Power Electronics, 2017, Volume: 32, Issue: 3. Pp. 2180 2188
- 15. Michael Cheah; Debashis Mandal; Bertan Bakkaloglu; Sayfe Kiaei, "A 100-mA, 99.11% Current Efficiency, 2-mVpp Ripple Digitally Controlled LDO With Active Ripple Suppression", Aug 2016.
- 16. Marti-Arbona, E.; Mandal, D.; Bakkaloglu, B.; Kiaei, S., "A High-Voltage Compliant Current-to-Digital Sensor for DC-DC Converters in Standard CMOS Technology," *IEEE Transactions on Power Electronics*, no. 99, 2016.
- 17. Chang, D.; Kitchen, J.N.; Bakkaloglu, B.; Kiaei, S.; Ozev, S., "Monitor-Based In-Field Wearout Mitigation for CMOS LC Oscillators," in *IEEE Transactions on Device and Materials Reliability*, vol. 16, no. 2, pp. 183-193, 2016.
- 18. Chang, D.; Kitchen, J.N.; Bakkaloglu, B.; Kiaei, S.; Ozev, S., "Design-Time Reliability Enhancement Using Hotspot Identification for RF Circuits," in *IEEE transactions on Very Large Scale Integration* (*VLSI*) *Systems*, -vol. 24, no. 3, pp. 1179-1183, 2016
- 19. Seungkee Min; Copani, T.; Kiaei, S.; Bakkaloglu, B., "A 90-nm CMOS 5-GHz Ring-Oscillator PLL With Delay-Discriminator-Based Active Phase-Noise Cancellation," *Solid-State Circuits, IEEE Journal of*, vol.48, no.5, pp.1151,1160, May 2013

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- 20. Junghan Lee; Tino Copani; Terry Mayhugh Jr.; Bhaskar Aravind; Sayfe Kiaei; Bertan Bakkaloglu.;, "A 280 mW, 0.07% THD+N class-D audio amplifier using a frequency-domain quantizer," *Analog Integrated Circuits and Signal Processing*, 173-186, 2012.
- 21. Seungkee Min; Copali, T.; Kiaei, S.; Bakkaloglu, B.; , "A 90nm CMOS 5GHz ring oscillator PLL with delay-discriminator based active phase noise cancellation," *Radio Frequency Integrated Circuits Symposium (RFIC)*, 2012 IEEE, pp. 173-176, 2012
- 22. Deligoz, I.; Naqvi, S.R.; Copani, T.; Kiaei, S.; Bakkaloglu, B.; Sang-Soo Je; Junseok Chae; , "A MEMS-Based Power-Scalable Hearing Aid Analog Front End," *Biomedical Circuits and Systems, IEEE Transactions on*, vol.5, no.3, pp.201-213, June 2011
- 23. Copani, T.; Seungkee Min; Shashidharan, S.; Chakraborty, S.; Stevens, M.; Kiaei, S.; Bakkaloglu, B.; , "A CMOS Low-Power Transceiver With Reconfigurable Antenna Interface for Medical Implant Applications," *Microwave Theory and Techniques, IEEE Transactions on*, vol.59, no.5, pp.1369-1378, May 2011
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- 72. "Compressed Vector-Based Spectral Analysis Technique for RF Nonlinear Analysis and Simulation of Circuits and Systems," Proc. of IEEE WAMI Conference, Clearwater, FL, June 2004. [S. Farahani, N. Darbanian, S. Kiaei]
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- 76. "Monolithic Supply Modulated RF Power Amplifier and DC-DC Power Converter IC," Proc. of 2003 IEEE MTT-S International, June 2003. [Abedinpour, S.; Deligoz, K.; Desai, J.; Figiel, M.; Kiaei, S.]
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- 97. "Fundamentals of ADSL system," SuperComm, Atlanta, GA, June 1998. [S. Kiaei]
- 98. "Low-Power RF Design," Design Automation Conference (DAC), Anaheim, CA, June 1997. [S. Kiaei]
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- 120. "Synthesis Techniques for CMOS Folded Source-Coupled Logic Circuits," IEEE Journal of Solid-State Circuits, Aug. 1992. [Maskai, S.R.; Kiaei, S.; Allstot, D.J.]
- 121. "A Folding Transformation for VLSI IIR Filter Array Design," Proc. of International Conference on Acoustics, Speech, and Signal Processing, Toronto, Canada, pp. 1237-1240, May 1991. [S. Rajopadhye, S. Kiaei]
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- 127. "VLSI Design of Bit/Serial Adaptive IIR Filters," Proc. of IEEE Pacific Conference on Communications, Computers, and Signal Processing, Victoria, Canada, pp. 650-652, June 1989. [R. Badyal, S. Kiaei]
- 128. "CCA Approach for ARMA Spectral Analysis," Proc. of IEEE International Symposium on Circuits and Systems, Portland, OR, pp. 1319-1322, May 1989. [S. Kiaei, L. Luo]
- 129. "Canonical Correlation Analysis (CCA) for ARMA Spectral Estimation," IEEE International Symposium on Circuits and Systems, May, 1989. [Kiaei, S.; Luo, L.]
- 130. "VLSI Implementation of Adaptive Bit/Serial IIR Filters," IEEE Pacific Rim Conference on Communications, Computers and Signal Processing, June 1989. [Badyal, R.; Kiaei, S.]
- 131. "VLSI design of WAP for Recursive Equations," VLSI Signal Processing, 1988. [S. Kiaei, U. Desai]
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- 133. "A Stochastic Realization Approach to Reduced-Order Hierarchical Estimation," Proc. of 24th IEEE Conference on Dec., Ft. Lauderdale, FL, pp. 416-421, December 1985. [U. Desai, S. Kiaei]
- 134. "Hierarchical Estimation Algorithms," Proc. of IEEE Conference on Man, Cybernetics, and Systems, Tucson, AZ, October 1985. [U. Desai S. Kiaei]
- 135. "Approximation of Markovian Models with Non-Constant Parameters," Proc. of 23rd IEEE Conference on Dec., Las Vegas, NV, pp. 1642-1644, December 1984. [U. Desai, S. Banerjee, S. Kiaei]
- 136. "A Canonical Correlation Approach to Reduced-Order LQR Design," Proc. of 23rd IEEE Conference on Dec., Las Vegas, NV, pp. 1523-1528, December 1984. [U. Desai, S. Banerjee, S. Kiaei]

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GRADUATE STUDENT ADVISEES & RESEARCH PROJECT

(Partial list of Students graduated, current employment to the best of my knowledge)

- 1. J. Durgam, VLSI Design of Dynamically Reconfigurable Array Processors, MSEE, 1988. Intel.
- 2. J. Gilbert, Minimization Techniques for PLAs, MSEE, 1988, Tektronix Inc.
- 3. L. Luo, CCA Methods for ARMA Spectral Estimation, MSEE, 1989. Berkeley Research Center
- 4. E. Zahl, Enhancement Methods for A/D Noise Reduction, MSEE, 1989. AT&T
- 5. L. Aihua, Synthesis of MRAs, MSEE, 1990. Intel.
- 6. F. Aslam, Image Restoration Methods, MSEE, 1990.
- 7. S.H. Chee, FSCL Circuits for Mixed-Mode IC's, MSEE, 1990. Linear Tech.
- 8. C. Dawson, MSEE, 1990. Boeing
- 9. A. Chow, Source-Coupled Logic ALU, MSEE, 1990. Intel
- 10. S. Maskai, Decimation Filters Using FSCL Circuits, MSEE, 1991. Intel
- 11. L. Louis, VLSI Implementation of Toeplitz Matrices, MSEE, 1991.
- 12. R. Badyal, Bit/Serial VLSI Design of IIR Filters, MSEE, 1992, HP
- 13. Lap Mui, Piece-Wise Linear Schedule for VLSI Arrays, MSEE, 1992. HP
- 14. S. Abdennadher, Adaptive Sigma-Delta Modulators, MSEE, 1992. Level One / Intel.
- 15. H. Bribech, Second Order Adaptive A/D Schemes, MSEE, 1992.
- 16. B. Hickman, MSEE, 92. Tektronix
- 17. M. Maleki, Current-Mode Flash A/D, MSEE, 1992. University of Oregon
- 18. Man Wong, Low-Noise Decimation Filter for Mixed-Mode ICs, MSEE, 1993, Motorola.
- 19. Anu Krishna Swamy, Low Noise IC Blocks for Mixed-mode IC's, MSEE, 1993, Ph.D., 1997.
- 20. Manu Srivastava, Comparison of Differential Logic (FSCL, CVSL, DSLL), MSEE, 1994, Intel.
- 21. Joel Oren, VLSI Design of Asynchronous FIR Filters, MSEE thesis, Feb. 1994. E-Systems.
- 22. Y. Zheng, VLSI Design and Synthesis of Multi-Rate Arrays, Ph.D. March 94, Hughes Research.
- 23. Satish Kulkarni, Low-Sensitivity Filters, MSEE, 1995, Motorola.
- 24. Amit Dutta, Multi-user Interference Cancellation, Ph.D, Dec. 97, Faculty, India.
- 25. Dwight Poplin, Multiplierless MPEG Decoder, MSEE, 1996. HP.
- 26. Maxim Scarpa, Adaptive I/Q Miss-match Correction for Direct Conversion Receivers, MSEE 1998.
- 27. Jeff McNeal, Sigma-Delta Frequency-to-Time Conversion, MSEE, 1998. Level One Comm.
- 28. Julia Vogel, Adaptive DC offset Cancellation, MSEE, 1998. Faculty in Germany.
- 29. Takao Inoue, MS, Echo Cancellation for ADSL, 1998. MSEE, The U of Texas at Austin.
- 30. Navid Lashkarian, Frequency off-set estimation and Synchronization of OFDM systems, Ph.D., June 1999. Broadcom Inc. & Faculty at UC San Jose.

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- 31. Guner Arslan, (co-advisor with B. Evans), "Fast Equalization for DMT systems, with applications to ADSL," Ph.D. The University of Texas at Austin, 2000
- 32. Salem Abdennadher, I/Q Mismatch Correction for RF Wireless transceivers, Ph.D., Level One Comm/Intel.
- 33. Can Sandalci, DSL Line Driver, Ph.D., 2001, Intel.
- 34. Dean Badillo, Low-Cost VCO Ring Oscillators, PhD, 2004, Intel, Chandler,
- 35. Siamak Abedinpour, PhD, 2005 Freescale, Tempe, Arizona
- 36. Hemanth Shivalingaiah, Multi-Band Low Noise Amplifiers, Ph.D., 2006, Intel,
- 37. Shahin Farahani, PhD, 2006, Qualcomm Inc,
- 38. Nazanin Darbanian, M.S. Freescale, Tempe, Arizona
- 39. Joe Rutkowski, Joseph, MS, 2004, Phillips.
- 40. Chaudhuri, Bikram, Synthesizer, MS/PhD, MS 2004.
- 41. Zhang, Jiandong, MEMs, MEMS, December-04
- 42. Afsahi, Ali, MS/PHD, UC San Diego, QUALCOMM, Connection One
- 43. Chen, Xiaomin, UWB, PHD, 2007, SRC/Motorola
- 44. Jali, Hilda, Power Management, MS, June-05,
- 45. Xuejin Wang, RF Optimization, 2006 CAD tools, PhD, Neo-Linear
- 46. Umar Lyles, Power Amplifier, MS, 2006. Texas Instruments
- 47. MS, Erika Munoz, RADHARD, 2007, Intel
- 48. Waleed Khali, (Co-Advisor), Professor at Ohio State
- 49. Jennifer Kitchen, PhD, 2009, Professor at ASU
- 50. Shahin Mehdizad Taleie, RFDAC, PhD, 2009, Qualcomm
- 51. Ilker Deligoz, PHD, 2009, Qualcomm
- 52. Hyung Kim, PhD, Jan 2010, Intel
- 53. Jung Le, PhD 2010, Intel, TI
- 54. Syed Naqvi, PhD, 2012, Intel.
- 55. Todd Martin, MS, 2011, TI
- 56. Seungkee Min, PhD, 2011, Intel
- 57. Ali Meamar, Post Doc, RFIC 2013
- 58. Hitesh Khunti, MS 2013, Qualcom
- 59. Debashis Mandal, Post Doc, Research faculty 2015-2018
- 60. Edgar Martinez, PhD, 2015, Qualcomm
- 61. Chirag Desai, MS, 2016, Qualcom
- 62. Sanjay Avasarala, MS, 2016

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- 63. Li Ming, MS, 2017
- 64. Qirong Peng, MS, 2017,
- 65. Yu Geng, PhD, 2018
- 66. Amir Ayati, PhD Aug 2018; Qualcomm
- 67. Pasisa Mahmoudi, PhD, May 2019, Qualcomm
- 68. Chai Yong, MS: 2015, PHD: 2019, Qualcomm
- 69. Shrikant Singh, MS: 2016, PhD, 2019, Movandi
- 70. Amir Alizadeh, Research Faculty 2019-Present
- 71. Ata S. PhD, 2021, Ata Sarrafinejad, PhD, 2021

UNIVERSITY COMMITTEES

Various Committees at ASU, Oregon State University, etc.

INDUSTRY COMMITTEES

- Arizona Telecommunications and Information Council (ATIC), Board Member
- CAS Fellows Committee (ends December 31, 2006)
- IEEE CAS Phoenix Chapter Organizers (the committee is in the process of determining new chair current chair not active)
- Executive Committee, RFIC 2006.
- Technical Program Comm, IEEE RFIC 2006.
- Executive Committee, Conferences, International Solid Sate System's Conference.
- IEEE CAS Society, VLSI Technical Comm. Member
- Editorial Board, IEEE Communications Surveys & Tutorials
- Radio Frequency Integrated Circuits- RFIC 2006
- IEEE RF Integrated Circuits Conference, Committee Chair for two workshops
- International Microwave Symposium, IMS-MTT 2006
- Int. Symposium on Circuits and Systems ISCAS 2006
- Wireless Networks & Emerging Technologies, WNET06
- Midwest Symposium on Circuits and System
- Arizona Governor IT Advisory Committee GITA
- Arizona Telecom ATIC

INSTRUCTIONAL SUMMARY

- Digital IC Design, Analog IC Design, Advance CMOS Analog IC, VLSI, RFIC Design
- Wireless Transceiver Design, Wireless Communications, GPS, Telecomm Systems, Digital Communication

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- Signal Processing, Advance digital signal processing, Communication, Digital Communication,
 Digital Audio Processing, Adaptive array processing
- Computer Architecture, Microprocessor System Architecture, Pipeline Array Processing